

**DHANALAKSHMI SRINIVASAN COLLEGE OF ENGINEERING
AND TECHNOLOGY**

**DEPARTMENT OF
ELECTRICAL AND ELECTRONICS ENGINEERING**

QUESTION BANK

III SEMESTER

EE8351 - DIGITAL LOGIC CIRCUITS

Regulation – 2017

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QUESTION BANK

SUBJECT : DIGITAL LOGIC CIRCUITS

SEM / YEAR: III/II

UNIT I - <u>NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES</u>				
Review of number systems, binary codes, error detection and correction codes (Parity and Hamming code) –Digital Logic Families- comparison of RTL, DTL, TTL, ECL and MOS families-operation, characteristics of digital logic family.				
PART – A				
Q.No	Questions		BT	Competence
1.	Convert (a) $(475.25)_8$ to its decimal equivalent (b) $(549.B4)_{16}$ to its binary equivalent		BTL1	Remember
2.	Define propagation delay.		BTL 1	Remember
3.	Determine $(377)_{10}$ in Octal and Hexa-Decimal equivalent.		BTL 2	Understand
4.	Compare the totem-pole output with open-collector output?		BTL 4	Analyze
5.	Give examples for weighted codes.		BTL 1	Remember
6.	What is meant by non-weighted codes?		BTL 1	Remember
7.	Convert 143_{16} into its binary and binary coded decimal equivalent.		BTL 1	Remember
8.	Convert 115_{10} and 235_{10} to hexadecimal numbers.		BTL 2	Understand
9.	List the factors used for measuring the performance of digital logic families.		BTL 2	Understand
10.	What is grey code and mention its advantages.		BTL 1	Remember
11.	Briefly explain the stream lined method of converting binary to decimal number with example.		BTL 5	Evaluate
12.	Give the Gray code for the binary number $(111)_2$		BTL 3	Apply
13.	When can RTL be used to represent digital systems?		BTL 3	Apply
14.	State the important characteristics of TTL family		BTL 3	Apply
15.	Convert (a) 1001001110101101_2 (b) 10010001011.00101110_2 to hexadecimal.		BTL 4	Analyze
16.	Summarize the advantages of ECL as compared to TTL logic family.		BTL 2	Understand
17.	Classify the basic families that belong to the bipolar families and to the MOS families.		BTL 5	Evaluate

18.	Which is faster TTL or ECL? Which requires more power to operate?		BTL 6	Create
19.	Define noise margin.		BTL 1	Remember
20.	Convert the following Excess 3 numbers into decimal numbers. (a)1011 (b)1001 0011 0111		BTL 6	Create
PART – B				
1.	(i) Perform the following addition using BCD and Excess-3 addition (205+569)	(7)	BTL 3	Apply
	(ii) Encode the binary word 1011 into seven bit even parity hamming code	(6)	BTL 6	Create
2.	(i) With circuit schematic, explain the operation of a two port TTL NAND gate with totem-pole output.	(8)	BTL 4	Analyze
	(ii) Compare totem pole and open collector outputs.	(5)	BTL 4	
3.	(i) Explain hamming code with an example. State its advantage over parity codes.	(7)	BTL 5	Evaluate
	(ii) Design a TTL logic circuit for a 3 input NAND gate.	(6)	BTL 5	
4.	Discuss about TTL parameters.	(13)	BTL 2	Understand
5.	With neat sketch explain the circuit diagram of CMOS NOR gate.	(13)	BTL 1	Remember
6.	Name and explain the characteristics of TTL family.	(13)	BTL 1	Remember
7.	Explain the characteristics and implementation of the following digital logic families. (a) CMOS (b) ECL (c) TTL	(4)	BTL 4	Analyze
		(6)		
		(3)		
8.	(i) Explain the classifications of binary codes. (ii) Explain about error detection and correction codes	(7)	BTL 5	Evaluate
		(6)	BTL 5	Evaluate
9.	(i) Assume that the even parity hamming code is 0110011 is transmitted and that 0100011 is received. The receiver does not know what is transmitted. Determine the bit location where error has occurred using received code. (ii) Draw the MOS logic circuit for NOT gate and explain its operation.	(7)	BTL 1	Remember
		(6)	BTL 1	Remember
10.	Write short notes on following: (a)RTL (b) DTL (c) TTL and (d) ECL	(13)	BTL 4	Analyze
11.	Explain in detail about error detection and error correcting codes.	(13)	BTL 3	Apply
12.	With neat sketch explain the operation of MOS family.	(13)	BTL 2	Understand

13.	(i) Perform the following addition using BCD and Excess-3 addition (502+965)	(7)	BTL 3	Apply
	(ii) Encode the binary word 1001 into seven bit even parity hamming code	(6)	BTL 6	Create
14.	(i) Design a odd parity hamming code generator and detector for 4-bit data and explain their logic.	(7)	BTL 2	Understand
	(ii) Convert FACE ₁₆ into its binary, octal, and decimal equivalent.	(6)		
PART – C				
1.	(i) Explain in detail the usage of hamming codes for error detection and error correction with an example considering the data bits as 0101	(12)	BTL 4	Analyze
	(ii) Convert 23.625 ₁₀ to octal(base 8)	(3)		
2.	(i) Using 16's complement method design the subtraction procedure and find C14 ₁₆ from 69B ₁₆	(8)	BTL 5	Evaluate
	(ii) Using 2's complement method design the subtraction procedure and find 110001 from 100101	(7)	BTL 5	
3.	(i) Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families.	(12)		
	(ii) Given the 2 binary numbers X=1010100 and Y=1000011 perform the subtraction Y-X by using 2's complements	(3)	BTL 5	Evaluate
4.	Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out power dissipation, propagation delay and noise margin. Compare its advantages over other logic families.	(15)	BTL 4	Analyse

UNIT II - <u>COMBINATIONAL CIRCUITS</u>				
Combinational logic- representation of logic functions- SOP and POS forms, K-map representations- minimization using K maps- simplification and implementation of combinational logic- multiplexers and de multiplexers- code converters, adders, subtractors, Encoders and Decoders.				
PART – A				
Q.No	Questions		BT	Competence
1.	Convert the given expression in canonical SOP form $Y=A'C+AB+BC'$		BTL 4	Remember
2.	Simplify the expression $Z=AB'+AB.(A'C)'$		BTL 3	Apply
3.	Given $F=B'+A'B+A'C'$: Identify the redundant term using K- map		BTL 4	Analyze
4.	Simplify : $xy+x'z+yz$		BTL 3	Apply
5.	Judge that (a) $a+a'b=a+b$; (b) $x'y'z+x'yz+xy'=x'z+xy'$		BTL 6	Create

6.	Write the POS form of the SOP expression $f(x,y,z) = x'yz + xyz' + xy'z$.		BTL 6	Create
7.	Draw the circuit of the function $F = \sum(0,6)$ with NAND gates		BTL 4	Analyze
8.	How does don't care condition in K-map help for circuit simplification?		BTL 5	Evaluate
9.	What are the basic digital logic gates?		BTL 1	Remember
10.	What is a Logic gate?		BTL 1	Remember
11.	Define combinational logic		BTL 1	Remember
12.	What is a karnaugh map? Interpret the limitations of karnaugh map.		BTL 2	Understand
13.	Construct OR gate using only NAND gates.		BTL 3	Apply
14.	What is meant by priority encoder?		BTL 2	Understand
15.	Draw the logic diagram of a half adder.		BTL 1	Remember
16.	Draw the truth table of 2:1 MUX		BTL 5	Evaluate
17.	Define multiplexer.		BTL 1	Remember
18.	What is the difference between decoder and demultiplexer?		BTL 2	Understand
19.	Why is MUX called as data selector?		BTL 2	Understand

20.	Design a half subtractor.		BTL 1	Remember
PART – B				
1.	(i) Explain briefly about SOP and POS forms with example. (ii) Plot the logical expression $ABCD + AB'C'D' + AB'C + AB$ on a 4 variable K-map. Obtain the simplified expression from the map.	(7) (6)	BTL 6 BTL 3	Create Apply
2.	(i) Reduce the following function using K-map $f(A,B,C,D) = \prod M(0,2,3,8,9,12,13,15)$ (ii) Minimize the function $F(a,b,c,d) = \sum(0,4,6,8,9,10,12)$ with $d = \sum(2,13)$. Implement the function using only NOR gates.	(7) (6)	BTL 1 BTL 4	Remember Analyze
3.	With the use of Maps, Find the simplest form in SOP of the function $F=f.g$, where f and g are given by $f = wxy' + y'z + w'yz' + x'yz'$ $g = (w+x+y'+z')(x'+y'+z)(w'+y+z')$	(13)	BTL 2	Understand
4.	(i) Prove that $F = A'.B + A.B'$ is exclusive OR operation and it equals $(((A.B)'.A)'.((A.B)'.B)')'$ (ii) Prove that for constructing XOR from NANDs we need four NAND GATES	(7) (6)	BTL 1 BTL 1	Remember Remember

5.	<p>(i) State and prove De-Morgan's theorem</p> <p>(ii) Simplify the following Boolean expression using K-map $f(x,y,z)=x y'z'+xyz+xyz'+x y' z+xyz'$</p> <p>$f(A,B,C,D)=\sum(0,1,5,6,7,10,12,14)+\sum(3,9)$</p>	(4)	BTL1	Remember
6.	<p>Reduce the Boolean function using k-map technique and implement using gates $f(w,x,y,z)=\sum m(0,1,4,8,9,10)$ which has the don't cares condition $d(w,x,y,z)=\sum m(2,11)$.</p>	(13)	BTL 2	Understand

7.	(i) Express the function $F=A+B C$ in Canonical SOP form & Canonical POS form	(7)	BTL 4	Analyse
	(ii) Simplify using K map $F(A,B,C,D)=\sum m(7,8,9)+d(10,11,12,13,14,15)$	(6)	BTL 2	Understand
8.	(i) Express the function $Y = A+B' C$ in canonical SOP and canonical POS form.	(7)	BTL 3	Apply
	(ii) Design BCD to Excess 3 code converter.	(6)	BTL 5	Evaluate
9.	(i) Implement the following Boolean function using 8:1 Mux: $F(A,B,C,D)=\sum m(0,1,3,4,8,9,15)$	(7)	BTL 1	Remember
	(ii) Design a full subtractor using half subtractors.	(6)	BTL 6	Create
10.	(i) Design a full adder using NOR gates	(7)	BTL 1	Remember
	(ii) Design a 3*8 decoder and explain its operation as a minterm generator.	(6)	BTL 1	Remember
11.	(i) Explain about combinational logic	(7)	BTL 4	Analyse
	(ii) Design a 3 bit magnitude comparator using gates	(6)	BTL 4	
12.	(i) Draw the logic diagram of a 4 bit carry look ahead adder and explain how this adder is advantageous over the ripple carry adder	(8)	BTL 4	Analyse
	(ii) Explain with the suitable example how a multiplexer is used to implement the Boolean function	(5)	BTL 4	
13.	(i) Write the step by step procedure for converting SOP and POS to standard SOP and POS forms.	(7)	BTL 3	Apply
	(ii) Design a 4-bit Binary to Gray code converter and implement it using logic gates.	(6)	BTL 3	
14.	(i) Design a full subtractor and implement it using logic gates.	(7)	BTL 4	Analyse
	(ii) Design a full adder using two half adders and an OR gate.	(6)	BTL 6	Create
PART – C				
1.	(i) Implement using NOR gates $Y=(AB+C')D+EF$	(8)	BTL 5	Evaluate
	(ii) Reduce and design the following function using K-map $f(A,B,C,D)=\prod M(0,3,4,7,8,10,12,14)+d(2,6)$	(7)	BTL 4	Analyse
2.	Simplify the logical expression using K-map in SOP and POS forms $F(A,B,C,D)=\sum m(0,2,3,6,7)+d(8,10,11,15)$	(15)	BTL 5	Evaluate
3.	(i) Reduce the following minterms using K-Map. $F(w,x,y,z) = \sum m(0,1,3,5,6,7,8,12,14) + \sum d(9,15)$.	(7)	BTL 6	Create
	(ii) Implement the following function using suitable multiplexer. $F(a,b,c) = \sum m(3,7,4,5)$.	(6)		
4.	Design a full adder using 4X1 multiplexer; also write its truth table and logical diagram.	(15)	BTL 6	Create

UNIT III - SYNCHRONOUS SEQUENTIAL CIRCUITS

**Sequential logic-SR, JK, D and T flip flops- level triggering and edge triggering
- counters- asynchronous and synchronous type-Modulo counters –Shift registers-
design of synchronous sequential circuits – Moore and Melay models - Counters, state
diagram; state reduction; state assignment.**

PART – A

Q.No	Questions		BT	Competence
1.	Convert T Flip Flop to D Flip Flop.		BTL 4	Analyze
2.	State the rules for state assignment.		BTL 1	Remember
3.	What is state assignment problem?		BTL 1	Remember
4.	What are the benefits of state reduction?		BTL 1	Remember
5.	Show how the JK flip-flop can be modified into a D flip-flop or a T flip-flop		BTL 3	Apply
6.	Differentiate Mealy and Moore models.		BTL 4	Analyse
7.	What are the disadvantages of asynchronous sequential circuit?		BTL 1	Remember
8.	Give the characteristic equation and state diagram of JK flip-flop.		BTL 2	Understand
9.	What is a self-starting counter?		BTL 4	Analyze
10.	Compare combinational and sequential circuits		BTL 5	Evaluate
11.	Examine the drawback of RS flip-flop?		BTL 3	Apply
12.	Implement T flip-flop using JK flip-flop.		BTL 3	Apply
13.	What is a preset table counter and ripple counter?		BTL 1	Remember
14.	Interpret the drawback of SR flip-flop?		BTL 2	Understand
15.	What is synchronous sequential circuit?		BTL 1	Remember
16.	What is meant by state assignment?		BTL 6	Create
17.	Define truth table for JK flip-flop.		BTL 2	Understand
18.	Give the characteristic equation and characteristic table of T flip flop.		BTL 5	Evaluate
19.	What is race around condition in flip-flops?		BTL 2	Understand
20.	Design the excitation table for JK flip-flop.		BTL 6	Create

PART – B

1.	<p>Design a counter for the following state diagram</p>	(13)	BTL 6	Create
2.	<p>Estimate a sequential circuit for the following state equations $A(t+1) = C \oplus D$; $B(t+1) = A$; $C(t+1) = B$; $D(t+1) = C$.</p>	(13)	BTL 2	Understand

3.	Explain the operation, state diagram and characteristics of T flip flop and master slave JK flip flop.	(13)	BTL 2	Understand
4.	(i) Draw the logic diagram of 4-bit synchronous counter. Explain the operation of the counter using the timing diagram (ii) Explain the universal shift register in detail	(7) (6)	BTL 4 BTL 4	Analyze
5.	(i) Construct a JK flip-flop using a JK flip-flop, a 2*1 MUX and an inverter. (ii) A sequential circuit has two JK flip-flop A and B, two inputs x and y, and one output z. the equations are $J_A = Bx + B'y'$; $K_A = B'xy'$ $J_B = A'x$; $K_B = A + xy'$ $Z = Ax'y' + Bx'y$. Draw the logic diagram and state table.	(7) (6)	BTL 1 BTL 1	Remember Remember
6.	(i) Estimate a sequential circuit with two D-flip-flops A and B and one output x. When x=0, the state of the circuit goes through the state transitions from 00 01 11 10 00 and repeats. (ii) Estimate mod 7 counter using D flip-flops.	(7) (6)	BTL 2 BTL 2	Understand
7.	A sequential circuit has two JK flip-flops A and B. The flip-flop input functions are: $J_A = B$; $J_B = x$ $K_A = Bx$; $K_B = A \oplus x$ (i) Draw the logic diagram of the circuit (ii) Tabulate the state table (iii) Draw the state diagram	(4) (6) (3)	BTL 1 BTL 1 BTL 1	Remember
8.	8. Using JK flip-flops, design a synchronous counter which counts in the sequence , 000,001,010,011,100,101,110,111,000	(13)	BTL 5	Evaluate
9.	Construct reduced state diagram for the following state diagram. 	(13)	BTL 3	Apply
10.	Design a 3 bit binary counter using T flip-flop.	(13)	BTL 3	Apply

11.	Using partitioning minimization procedure reduce the following state table:			(13)	BTL 2	Understand		
	PRESENT STATE	NEXT STATE					OUTPUT	
		W=0	W=1				Z	
	A	B	C				1	
	B	D	F				1	
	C	F	E				0	
	E	F	C				0	
F	E	D	0					
12.	Differentiate asynchronous and synchronous type counters.			(13)	BTL 2	Understand		
13.	(i) Draw and explain the operation of Master-Slave JK flipflop			(7)	BTL 4	Create		
	(ii) Design a 5-bit ring counter and mention its applications.			(6)				
14.	Illustrate about 4-bit BCD ripple counters.			(13)	BTL 4	Analyze		
PART – C								
1.	What is meant by race-around condition? Discuss in detail about master-slave JK flip flop.			(15)	BTL 5	Evaluate		
2.	Design a sequential circuit using T-flip-flop. The state table of the circuit is as given below.			(15)	BTL 6	Create		
	PRESENT STATE	NEXT STATE					OUTPUT	
		x=0	x=1				x=0	x=1
	a	b	c				0	0
	b	f	e				0	0
	c	d	a				1	0
	d	g	c				0	0
e	f	b	1	1				
f	g	h	0	1				
g	g	a	1	0				
h	g	a	1	0				
3.	Explain in detail about different shift registers.			(15)	BTL 4	Analyse		
4.	(i) Explain the realisation of JK flipflop from T flipflop			(15)	BTL 6	Create		
	(ii) Write short notes on SIPO and draw the output waveforms.							

**UNIT IV - ASYNCHRONOUS SYNCHRONOUS SEQUENTIAL CIRCUITS AND
PROGRAMMABLE LOGIC DEVICES**

Asynchronous sequential logic circuits- Transition table, flow table-race conditions, hazards & errors in digital circuits; analysis of asynchronous sequential logic circuits-introduction to Programmability Logic Devices: PROM-PLA-PAL,CPLD-FPGA.

PART - A

Q.No	Questions		BT Level	Competence
1.	Define racing		BTL-1	Remember
2.	What is critical race?		BTL-1	Remember
3.	What is meant by transition table?		BTL-1	Remember
4.	Estimate the types of hazards		BTL-5	Evaluate
5.	What is the difference between flow table and transition table?		BTL-4	Analyze
6.	Define races in Asynchronous sequential circuit.		BTL-1	Remember
7.	Predict the hazards in asynchronous sequential circuits?		BTL-2	Understand
8.	Show what is fundamental mode of operation in asynchronous sequential circuits?		BTL-3	Apply
9.	What is static hazard and dynamic hazard?		BTL-4	Analyze
10.	Define asynchronous sequential machine.		BTL-1	Remember
11.	Predict what is a PROM?		BTL-5	Evaluate
12.	State the difference between static 0 and static 1 hazard		BTL-2	Understand
13.	Compose about secondary variable and excitation variables.		BTL-6	Create
14.	Compare critical race and non critical race.		BTL-3	Apply
15.	What is flow table? Give example.		BTL-6	Create
16.	What is a deadlock condition?		BTL-1	Remember
17.	Deduce the demerits in designing asynchronous sequential machines.		BTL-2	Understand
18.	State the difference between PROM, PAL, PLA and EPROM.		BTL-3	Apply

19.	What is a PLA?		BTL-2	Understand
20.	Point out the definition for flow table in asynchronous sequential circuit.		BTL-4	Analyze
PART B				
1.	Design an asynchronous sequential circuit has two inputs X_2 and X_1 and one output Z . When $X_1=0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.	(13)	BTL-6	Create
2.	(i) Implement the following function using PLA: $F(x,y,z) = \sum m(1,2,4,6)$ (ii) For the given Boolean function, obtain the hazard-free circuit. $F(A,B,C,D)=\sum m(1,3,6,7,13,15)$	(7) (6)	BTL-5	Evaluate
3.	(i) Obtain the PLA program table for a combinational circuit that squares a 3 bit number. Minimize the number of product terms. (ii) A combinational circuit is defined by the functions. (a) $F_1(a,b,c)=\sum m(3,5,6,7)$ (b) $F_2(a,b,c)=\sum m(0,2,4,5,7)$	(7) (6)	BTL-1 BTL-2	Remember Understand
4.	Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples.	(13)	BTL-4	Analyze
5.	Describe with reasons, the effect of races in asynchronous sequential circuit design. Explain its types with illustrations. Show the method of race-free state assignments with examples.	(13)	BTL-2	Understand
6.	(i) Discover asynchronous BCD counter using JK flip-flops. (ii) An asynchronous sequential circuit is described by $Y=x_1x_2+(x_1+x_2)y$; $z=y$. Draw the logic diagram, transition table and output map.	(7) (6)	BTL-1 BTL-4	Remember Analyze
7.	(i) Find a circuit that has no static hazards and implement Boolean function $F(A,B,C,D)=\sum(0,2,6,7,8,10,12)$ (ii) Explain the different types of programmable logic devices with neat sketch and compare them.	(7) (6)	BTL-2 BTL-4	Understand Analyze
8.	Derive the transition table and primitive flow table for the functional mode asynchronous sequential circuit shown in fig	(13)	BTL-2	Understand

9.	<p>Implement the following function in PLA</p> <p>(i) $F_1 = \sum m(1,2,4,6)$; $F_2 = \sum m(0,1,6,7)$; $F_3 = \sum m(2,6)$</p> <p>(ii) $F_1 = \sum m(3,5,8,9)$; $F_2 = \sum m(2,3,5,8,9)$; $F_3 = \sum m(0,1)$</p>	(7)	BTL-3	Apply
10.	<p>(i) Illustrate the following logic and analyse for the presence of any hazard $f = x_1x_2 + x_1'x_3$. If hazard is present briefly explain the type of hazard and design a hazard-free circuit.</p> <p>(ii) Illustrate the following function in PLA</p> $f_1(x,y,z) = \sum m(0,1,3,5,7)$ $f_2(x,y,z) = \sum m(2,4,6)$	(7)	BTL-4	Analyze
11.	Discover an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T=1 & C moves from 1 to 0. Otherwise the output is 0.	(13)	BTL-1	Remember
12.	Discover an asynchronous BCD counter.	(13)	BTL-1	Remember
13.	Describe the steps involved in design of asynchronous sequential circuit in detail with an example.	(13)	BTL-3	Apply
14.	<p>(i) How do you get output specifications from a flow table in asynchronous sequential circuit operating in fundamental mode?</p> <p>(ii) When do you get the critical and non-critical races? How will you obtain race free conditions?</p>	(4)	BTL-1	Remember
		(9)	BTL-1	Remember
PART C				

1.	(i) Design a PLA structure using AND and OR logic for the following function. $F1 = \sum m(0,1,2,3,4,7,8,11,12,15)$ $F2 = \sum m(2,3,6,7,8,9,12,13)$ $F3 = \sum m(1,3,7,8,11,12,15)$ $F4 = \sum m(0,1,4,8,11,12,15)$ (ii) Compare PLA and PAL Circuits	(12)	BTL-6	Create
		(3)	BTL-2	Understand
2.	A combinational circuit is defined by the functions $F1 = \sum m(3,5,6,7)$ and $F2 = \sum m(0,2,4,7)$. Implement the circuit with PLA and PAL design.	(15)	BTL-6	Create
3.	Design an asynchronous circuit that has two inputs x_1 and x_2 and one output z . the circuit is required to give an output whenever the input sequence (0,0),(0,1) and (1,1) received but only in that order.	(15)	BTL-6	Create
4.	An asynchronous sequential circuit is described by the following excitation and the output function $Y = x_1x_2 + (x_1 + x_2)y$. (i) Draw the logic diagram of the circuit. (ii) Derive the transition table and output map. (iii) Describe the behaviour of the circuit.	(4)	BTL-4	Analyze
		(8)		
		(3)		

UNIT V - VHDL

RTL Design –combinational logic –Sequential circuit –Operators –Introduction to Packages – Subprograms– Test bench. (Simulation/Tutorial Examples: adders, counters, flip flops, Multiplexers & De multiplexers).

PART - A

Q.No	Questions		BT	Competence
1.	What is a package in VHDL?		BTL-1	Remember
2.	Write the VHDL behavioural model for D-flip-flop.		BTL-1	Remember
3.	Write the VHDL code for a logical gate which gives high output only when both the inputs are high.		BTL-1	Remember
4.	Name any four hardware description language test benches.		BTL-1	Remember
5.	Give the syntax for package declaration and package body in VHDL		BTL-1	Remember
6.	Write VHDL code for 2*1 MUX using behavioural modeling		BTL-1	Remember
7.	Deduce what is test bench?		BTL-4	Analyze
8.	Compose the operators used in VHDL		BTL-6	Create
9.	Compile VHDL code for half adder in data flow model.		BTL-6	Create
10.	Analyze the merits of hardware languages.		BTL-5	Evaluate
11.	What is the function of wait statement in VHDL package?		BTL-2	Understand
12.	Predict the need for VHDL.		BTL-4	Analyze
13.	Prepare the VHDL code for AND gate.		BTL-5	Evaluate
14.	Give the test bench for AND gate.		BTL-2	Understand
15.	Show the meaning of the following RTL statement?		BTL-3	Apply
16.	Categorize different test bench.		BTL-4	Analyze
17.	What is subprogram overloading?		BTL-2	Understand
18.	Expand the following acronyms. (a)VHDL (b)VHLSI		BTL-3	Apply
19.	What are the languages that are combined together to get VHDL language?		BTL-3	Apply
20.	Write the VHDL code for full subtractor in data flow model.		BTL-2	Understand
PART - B				
1.	Write the VHDL code to realize a full adder using (i) Behavioral modeling. (ii) Structural modeling.	(7+6)	BTL-1	Remember

2.	Write the VHDL code to realize a 3-bit gray code counter using case statement.	(13)	BTL-1	Remember
3.	Write VHDL code for Binary UP/ DOWN counter using JK flip-flops.	(13)	BTL-1	Remember
4.	Design a 3 bit magnitude comparator and write the VHDL coding to realize it using structural modelling.	(13)	BTL-2	Understand
5.	(i) Explain the digital system design flow sequence with the help of a flow chart. (ii) Estimate a VHDL code for a 4 bit universal shift register.	(7) (6)	BTL-4 BTL-4	Analyze Analyze
6.	Explain in detail the concept of Structural modelling in VHDL with an example of full adder.	(13)	BTL-5	Evaluate
7.	(i) Explain in detail the various programming constructs used in VHDL for designing a logic circuit. (ii) Discuss the various packages. Write a VHDL code for the implementation of decoder/de-multiplexer.	(7) (6)	BTL-4 BTL-4	Analyze Analyze
8.	(i) Write VHDL code for 4 bit synchronous UP/DOWN counter and explain. ii) Write short notes on subprograms used for implementation of adders.	(8) (5)	BTL-1 BTL-1	Remember Remember
9.	Design a VHDL code for full adder and 8*1 MUX	(13)	BTL-6	Create
10.	Illustrate the VHDL code for JK master slave flip-flops and using JK FF as structural elements write code for 4 bit asynchronous counter.	(5+8)	BTL-4	Analyze
11.	Interpret the structural VHDL description for a 2 to 4 decoder in detail.	(13)	BTL-3	Apply
12.	Discover a VHDL code for 6 bit comparator and also explain the design procedure.	(13)	BTL-2	Understand
13.	Discover a VHDL code for 4 bit binary counter with parallel load and explain.	(13)	BTL-2	Understand
14.	(i) Explain the design procedure of RTL using VHDL. (ii) Write a note on VHDL test benches.	(8) (5)	BTL-3 BTL-3	Apply Apply
PART - C				
1.	Design a 4 X 4 array multiplier and write the VHDL coding to realize it using structural modelling.	(15)	BTL-6	Create
2.	(i) Discover the VHDL code for 3 to 8 decoder. (ii) Discover the VHDL code for 4:1 multiplexer.	(8) (7)	BTL-6	Create

3.	(i) Discuss briefly the packages in VHDL (ii) Write an VHDL coding for realization of clocked S-R flip flop.	(7) (8)	BTL-5	Evaluate
4.	i) Write short notes on built-in operators used in VHDL programming. ii) Write VHDL coding for 4 X 1 Multiplexer	(7) (8)	BTL-3	Apply