**DHANALAKSHMI SRINIVASAN COLLEGE OF ENGINEERING**

 **AND TECHNOLOGY**

**DEPARTMENT OF**

**ELECTRICAL AND ELECTRONICS ENGINEERING**

QUESTION BANK

III SEMESTER

EE8351 - DIGITAL LOGIC CIRCUITS

Regulation – 2017

Academic Year 2018-2019

**QUESTION BANK SUBJECT : DIGITAL LOGIC CIRCUITS**

**SEM / YEAR: III/II**

|  |  |
| --- | --- |
|  | **UNIT I - NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES** |
|  | **Review of number systems, binary codes, error detection and correction codes (Parity and Hamming code) –Digital Logic Families- comparison of RTL, DTL, TTL, ECL and MOS families-operation, characteristics of digital logic family.** |
|  | **PART – A** |
| **Q.No** | **Questions** |  | **BT** | **Competence** |
| 1. | Convert1. (475.25)8 to its decimal equivalent
2. (549.B4)16 to its binary equivalent
 |  | **BTL1** | **Remember** |
| 2. | Define propagation delay. |  | **BTL 1** | **Remember** |
| 3. | Determine (377)10 in Octal and Hexa-Decimal equivalent. |  | **BTL 2** | **Understand** |
| 4. | Compare the totem-pole output with open-collector output? |  | **BTL 4** | **Analyze** |
| 5. | Give examples for weighted codes. |  | **BTL 1** | **Remember** |
| 6. | What is meant by non-weighted codes? |  | **BTL 1** | **Remember** |
| 7. | Convert 14316 into its binary and binary coded decimalequivalent. |  | **BTL 1** | **Remember** |
| 8. | Convert 11510 and 23510 to hexadecimal numbers. |  | **BTL 2** | **Understand** |
| 9. | List the factors used for measuring the performance of digital logic families. |  | **BTL 2** | **Understand** |
| 10. | What is grey code and mention its advantages. |  | **BTL 1** | **Remember** |
| 11. | Briefly explain the stream lined method of converting binary to decimal number with example. |  | **BTL 5** | **Evaluate** |
| 12. | Give the Gray code for the binary number (111)2 |  | **BTL 3** | **Apply** |
| 13. | When can RTL be used to represent digital systems? |  | **BTL 3** | **Apply** |
| 14. | State the important characteristics of TTL family |  | **BTL 3** | **Apply** |
| 15. | Convert (a) 10010011101011012(b) 10010001011.001011102 to hexadecimal. |  | **BTL 4** | **Analyze** |
| 16. | Summarize the advantages of ECL as compared to TTL logic family. |  | **BTL 2** | **Understand** |
| 17. | Classify the basic families that belong to the bipolar families and to the MOS families. |  | **BTL 5** | **Evaluatee** |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 18. | Which is faster TTL or ECL? Which requires more power to operate? |  | **BTL 6** | **Create** |
| 19. | Define noise margin. |  | **BTL 1** | **Remember** |
| 20. | Convert the following Excess 3 numbers into decimal numbers.(a)1011 (b)1001 0011 0111 |  | **BTL 6** | **Create** |
|  | **PART – B** |
| 1. | 1. Perform the following addition using BCD and Excess-3 addition (205+569)
2. Encode the binary word 1011 into seven bit even parity hamming code
 | (7)(6) | **BTL 3****BTL 6** | **Apply****Create** |
| 2. | 1. With circuit schematic, explain the operation of a two port TTL NAND gate with totem-pole output.
2. Compare totem pole and open collector outputs.
 | (8)(5) | **BTL 4****BTL 4** | **Analyze** |
| 3. | 1. Explain hamming code with an example. State its advantage over parity codes.
2. Design a TTL logic circuit for a 3 input NAND gate.
 | (7)(6) | **BTL 5****BTL 5** | **Evaluate** |
| 4. | Discuss about TTL parameters. | (13) | **BTL 2** | **Understand** |
| 5. | With neat sketch explain the circuit diagram of CMOSNOR gate. | (13) | **BTL 1** | **Remember** |
| 6. | Name and explain the characteristics of TTL family. | (13) | **BTL 1** | **Remember** |
| 7. | Explain the characteristics and implementation of the following digital logic families.(a) CMOS (b) ECL (c) TTL | (4)(6)(3) | **BTL 4** | **Analyze** |
| 8. | (i)Explain the classifications of binary codes. (ii)Explain about error detection and correction codes | (7)(6) | **BTL 5****BTL 5** | **Evaluate Evaluate** |
| 9. | 1. Assume that the even parity hamming code is 0110011 is transmitted and that 0100011 is received. The receiver does not know what is transmitted. Determine the bit location where error has occurred using received code.
2. Draw the MOS logic circuit for NOT gate and explain its operation.
 | (7)(6) | **BTL 1****BTL 1** | **Remember****Remember** |
| 10. | Write short notes on following:(a)RTL (b) DTL (c) TTL and (d) ECL | (13) | **BTL 4** | **Analyze** |
| 11. | Explain in detail about error detection and error correcting codes. | (13) | **BTL 3** | **Apply** |
| 12. | With neat sketch explain the operation of MOS family. | (13) | **BTL 2** | **Understand** |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 13. | 1. Perform the following addition using BCD and Excess-3 addition (502+965)
2. Encode the binary word 1001 into seven bit even parity hamming code
 | (7)(6) | **BTL 3****BTL 6** | **Apply****Create** |
| 14. | 1. Design a odd parity hamming code generator and detector for 4-bit data and explain their logic.
2. Convert FACE16 into its binary, octal, and decimal equivalent.
 | (7)(6) | **BTL 2** | **Understand** |
|  | **PART – C** |
|  | (i) Explain in detail the usage of hamming codes for error | (12) | **BTL 4** | **Analyze** |
| 1. | detection and error correction with an example considering the data bits as 0101 |  |  |  |
|  | (ii) Convert 23.62510 to octal(base 8) | (3) |  |  |
|  | (i) Using 16’s complement method design the subtraction | (8) | **BTL 5** | **Evaluate** |
| 2. | procedure and find C1416 from 69B16 |  |  |  |
|  | (ii) Using 2’s complement method design the subtraction | (7) | **BTL 5** |  |
|  | procedure and find 110001 from 100101 |  |  |  |
|  | (i) Explain with an aid of circuit diagram the operation of |  |  |  |
|  | 2 input CMOS NAND gate and list out its advantages over | (12) |  |  |
| 3. | other logic families.(ii) Given the 2 binary numbers X=1010100 and | (3) | **BTL 5** | **Evaluate** |
|  | Y=1000011 perform the subtraction Y-X by using 2’s |  |  |  |
|  | complements |  |  |  |
| 4. | Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out power dissipation, propagation delay and noise margin. Compare its advantages over other logic families. | (15) | **BTL 4** | **Analyse** |

|  |  |
| --- | --- |
|  | **UNIT II - COMBINATIONAL CIRCUITS** |
|  | **Combinational logic- representation of logic functions- SOP and POS forms, K- map representations- minimization using K maps- simplification and implementation of combinational logic- multiplexers and de multiplexers- code converters, adders, subtractors, Encoders and Decoders.** |
|  | **PART – A** |
| **Q.No** | **Questions** |  | **BT** | **Competence** |
| 1. | Convert the given expression in canonical SOP formY=A’C+AB+BC’ |  | **BTL 4** | **Remember** |
| 2. | Simplify the expression Z=AB’+AB.(A’C’)’ |  | **BTL 3** | **Apply** |
| 3. | Given F=B’+A’B+A’C’ : Identify the redundant term using K- map |  | **BTL 4** | **Analyze** |
| 4. | Simplify : xy+x’z+yz |  | **BTL 3** | **Apply** |
| 5. | Judge that (a) a+a’b=a+b; (b) x’y’z+x’yz+xy’=x’z+xy’ |  | **BTL 6** | **Create** |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 6. | Write the POS form of the SOP expression f(x,y,z) = x’yz + xyz’ + xy’z. |  | **BTL 6** | **Create** |
| 7. | Draw the circuit of the function F=∑(0,6) with NAND gates |  | **BTL 4** | **Analyze** |
| 8. | How does don’t care condition in K-map help for circuitsimplification? |  | **BTL 5** | **Evaluate** |
| 9. | What are the basic digital logic gates? |  | **BTL 1** | **Remember** |
| 10. | What is a Logic gate? |  | **BTL 1** | **Remember** |
| 11. | Define combinational logic |  | **BTL 1** | **Remember** |
| 12. | What is a karnaugh map? Interpret the limitations of karnaugh map. |  | **BTL 2** | **Understand** |
| 13. | Construct OR gate using only NAND gates. |  | **BTL 3** | **Apply** |
| 14. | What is meant by priority encoder? |  | **BTL 2** | **Understand** |
| 15. | Draw the logic diagram of a half adder. |  | **BTL 1** | **Remember** |
| 16. | Draw the truth table of 2:1 MUX |  | **BTL 5** | **Evaluate** |
| 17. | Define multiplexer. |  | **BTL 1** | **Remember** |
| 18. | What is the difference between decoder and demultiplexer? |  | **BTL 2** | **Understand** |
| 19. | Why is MUX called as data selector? |  | **BTL 2** | **Understand** |
| 20. | Design a half subtractor. |  | **BTL 1** | **Remember** |
|  | **PART – B** |
|  | (i) Explain briefly about SOP and POS forms with | (7) | **BTL 6** | **Create** |
| 1. | example.(ii) Plot the logical expression ABCD + AB’ C’ D’ + AB’C + AB on a 4 variable K-map. Obtain the simplified | (6) | **BTL 3** | **Apply** |
|  | expression from the map. |  |  |  |
|  | (i)Reduce the following function using K-map | (7) | **BTL 1** | **Remember** |
|  | f(A,B,C,D)=ΠM(0,2,3,8,9,12,13,15) |  |  |  |
| 2. | (ii) Minimize the function F(a,b,c,d)=∑(0,4,6,8,9,10,12) with d=∑(2,13). Implement the function using only NOR gates. | (6) | **BTL 4** | **Analyze** |
| 3. | With the use of Maps, Find the simplest form in SOP of the function F=f.g, where f and g are given byf = wxy’+y’z+w’yz’+x’yz’g= (w+x+y’+z’)(x’+y’+z)(w’+y+z’) | (13) | **BTL 2** | **Understand** |
|  | (i)Prove that F=A’.B+A.B’ is exclusive OR operation and | (7) | **BTL 1** | **Remember** |
| 4. | it equals = (((A.B)’.A)’.((A.B)’.B)’)’(ii) Prove that for constructing XOR from NANDs we need four NAND GATES | (6) | **BTL 1** | **Remember** |
|  | (i) State and prove De-Morgan’s theorem | (4) | **BTL1** | **Remember** |
| 5. | (ii) Simplify the following Boolean expression using K-map f (x,y,z)=x y’z’+xyz+xyz’~~+~~x y’ z+xyz’ | (9) | **BTL 1** | **Remember** |
|  | f(A,B,C,D)=∑(0,1,5,6,7,10,12,14)+∑(3,9) |  |  |  |
| 6. | Reduce the Boolean function using k-map technique and implement using gates f(w,x,y,z)= ∑m(0,1,4,8,9,10) which has the don’t cares condition d(w,x,y,z)= ∑m(2,11). | (13) | **BTL 2** | **Understand** |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | (i)Express the function F=A+B C in Canonical SOP form | (7) | **BTL 4** | **Analyse** |
| 7. | & Canonical POS form(ii) Simplify using K map F(A,B,C,D)=∑m(7,8,9)+d(10,11,12,13,14,15) | (6) | **BTL 2** | **Understand** |
|  | (i)Express the function Y = A+B’ C in canonical SOP and | (7) | **BTL 3** | **Apply** |
| 8. | canonical POS form.(ii) Design BCD to Excess 3 code converter. | (6) | **BTL 5** | **Evaluate** |
|  | (i) Implement the following Boolean function using 8:1 | (7) | **BTL 1** | **Remember** |
| 9. | Mux: F(A,B,C,D)=∑m(0,1,3,4,8,9,15)(ii)Design a full subtractor using half subtractors. | (6) | **BTL 6** | **Create** |
|  | (i) Design a full adder using NOR gates |  | **BTL 1** | **Remember** |
| 10. | (ii)Design a 3\*8 decoder and explain its operation as a minterm generator. | (7)(6) | **BTL 1** | **Remember** |
| 11. | 1. Explain about combinational logic
2. Design a 3 bit magnitude comparator using gates
 | (7)(6) | **BTL 4****BTL 4** | **Analyse** |
|  | 1. Draw the logic diagram of a 4 bit carry look ahead adder and explain how this adder is advantageous over the ripple carry adder
2. Explain with the suitable example how a multiplexer is used to implement the Boolean function
 | (8) | **BTL 4** | **Analyse** |
| 12. | (5) | **BTL 4** |  |
| 13. | 1. Write the step by step procedure for converting SOP and POS to standard SOP and POS forms.
2. Design a 4-bit Binary to Gray code converter and implement it using logic gates.
 | (7)(6) | **BTL 3****BTL 3** | **Apply** |
|  | (i) Design a full subtractor and implement it using logic | (7) | **BTL 4** | **Analyze** |
| 14. | gates.(ii) Design a full adder using two half adders and an OR | (6) | **BTL 6** | **Create** |
|  | gate. |  |  |  |
|  | **PART – C** |
| 1. | 1. Implement using NOR gates Y=(AB+C’)D+EF
2. Reduce and design the following function using K- map f(A,B,C,D)= ΠM(0,3,4,7,8,10,12,14)+d(2,6)
 | (8)(7) | **BTL 5****BTL 4** | **Evaluate Analyze** |
| 2. | Simplify the logical expression using K-map in SOP and POS forms F(A,B,C,D)= ∑m(0,2,3,6,7)+d(8,10,11,15) | (15) | **BTL 5** | **Evaluate** |
|  | (i) Reduce the following minterms using K-Map. | (7) | **BTL 6** | **Create** |
| 3. | F(w,x,y,z) = ∑m (0,1,3,5,6,7,8,12,14) + ∑d (9,15).(ii)Implement the following function using suitable multiplexer. F(a,b,c) = ∑m(3,7,4,5). | (6) |  |  |
| 4. | Design a full adder using 4X1 multiplexer; also write its truth table and logical diagram. | (15) | **BTL 6** | **Create** |

|  |  |
| --- | --- |
|  | **UNIT III - SYNCHRONOUS SEQUENTIAL CIRCUITS** |
|  | **Sequential logic-SR, JK, D and T flip flops- level triggering and edge triggering****- counters- asynchronous and synchronous type-Modulo counters –Shift registers- design of synchronous sequential circuits – Moore and Melay models - Counters, state diagram; state reduction; state assignment.** |
|  | **PART – A** |
| **Q.No** | **Questions** |  | **BT** | **Competence** |
| 1. | Convert T Flip Flop to D Flip Flop. |  | **BTL 4** | **Analyze** |
| 2. | State the rules for state assignment. |  | **BTL 1** | **Remember** |
| 3. | What is state assignment problem? |  | **BTL 1** | **Remember** |
| 4. | What are the benefits of state reduction? |  | **BTL 1** | **Remember** |
| 5. | Show how the JK flip-flop can be modified into a D flip-flop or a T flip-flop |  | **BTL 3** | **Apply** |
| 6. | Differentiate Mealy and Moore models. |  | **BTL 4** | **Analyse** |
| 7. | What are the disadvantages of asynchronous sequentialcircuit? |  | **BTL 1** | **Remember** |
| 8. | Give the characteristic equation and state diagram of JKflip-flop. |  | **BTL 2** | **Understand** |
| 9. | What is a self-starting counter? |  | **BTL 4** | **Analyze** |
| 10. | Compare combinational and sequential circuits |  | **BTL 5** | **Evaluate** |
| 11. | Examine the drawback of RS flip-flop? |  | **BTL 3** | **Apply** |
| 12. | Implement T flip-flop using JK flip-flop. |  | **BTL 3** | **Apply** |
| 13. | What is a preset table counter and ripple counter? |  | **BTL 1** | **Remember** |
| 14. | Interpret the drawback of SR flip-flop? |  | **BTL 2** | **Understand** |
| 15. | What is synchronous sequential circuit? |  | **BTL 1** | **Remember** |
| 16. | What is meant by state assignment? |  | **BTL 6** | **Create** |
| 17. | Define truth table for JK flip-flop. |  | **BTL 2** | **Understand** |
| 18. | Give the characteristic equation and characteristic table of Tflip flop. |  | **BTL 5** | **Evaluate** |
| 19. | What is race around condition in flip-flops? |  | **BTL 2** | **Understand** |
| 20. | Design the excitation table for JK flip-flop. |  | **BTL 6** | **Create** |
|  | **PART – B** |
| 1. | Design a counter for the following state diagram | (13) | **BTL 6** | **Create** |
| 2. | Estimate a sequential circuit for the following stateequations A(t+1)= C⊕D; B(t+1) = A; C(t+1) = B; D(t+1)=C. | (13) | **BTL 2** | **Understand** |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 3. | Explain the operation, state diagram and characteristics of T flip flop and master slave JK flip flop. | (13) | **BTL 2** | **Understand** |
| 4. | 1. Draw the logic diagram of 4-bit synchronous counter. Explain the operation of the counter using the timing diagram
2. Explain the universal shift register in detail
 | (7)(6) | **BTL 4****BTL 4** | **Analyze** |
| 5. | 1. Construct a JK flip-flop using a JK flip-flop, a 2\*1 MUX and an inverter.
2. A sequential circuit has two JK flip-flop A and B, two inputs x and y, and one output z. the equations are JA=Bx+B’y’; KA= B’xy’

JB= A’x; KB=A+xy’Z=Ax’y’+Bx’y.Draw the logic diagram and state table. | (7)(6) | **BTL 1****BTL 1** | **Remember****Remember** |
| 6. | 1. Estimate a sequential circuit with two D-flip-flops A and B and one output x. When x=0, the state of the circuit goes through the state transitions from 00 01 11 10 00

and repeats.1. Estimate mod 7 counter using D flip-flops.
 | (7)(6) | **BTL 2****BTL 2** | **Understand** |
| 7. | A sequential circuit has two JK flip-flops A and B. The flip- flop input functions are:JA=B; JB=xKA= B x ; KB=A⊕x(i)Draw the logic diagram of the circuit (ii)Tabulate the state table(iii)Draw the state diagram | (4)(6)(3) | **BTL 1****BTL 1****BTL 1** | **Remember** |
| 8. | 8. Using JK flip-flops, design a synchronous counter which counts in the sequence , 000,001,010,011,100,101,110,111,000 | (13) | **BTL 5** | **Evaluate** |
| 9. | Construct reduced state diagram for the following state diagram. | (13) | **BTL 3** | **Apply** |
| 10. | Design a 3 bit binary counter using T flip-flop. | (13) | **BTL 3** | **Apply** |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 11. | Using partitioning minimization procedure reduce the following state table: | (13) | **BTL 2** | **Understand** |
|  | PRESENT STATE | NEXT STATE | OUTPUT |  |
| W=0 | W=1 | Z |
| A | B | C | 1 |
| B | D | F | 1 |
| C | F | E | 0 |
| E | F | C | 0 |
| F | E | D | 0 |
| 12. | Differentiate asynchronous and synchronous type counters. | (13) | **BTL 2** | **Understand** |
| 13. | 1. Draw and explain the operation of Master-Slave JK flipflop
2. Design a 5-bit ring counter and mention its applications.
 | (7)(6) | **BTL 4** | **Create** |
| 14. | Illustrate about 4-bit BCD ripple counters. | (13) | **BTL 4** | **Analyze** |
|  | **PART – C** |
| 1. | What is meant by race-around condition? Discuss in detail about master and slave JK flipflop | (15) | **BTL 5** | **Evaluate** |
| 2. | Design a sequential circuit using T-flip-flop. The state table of the circuit is as given below. | (15) | **BTL 6** | **Create** |
| 3. | Explain in detail about different shift registers. | (15) | **BTL 4** | **Analyse** |
| 4. | 1. Explain the realisation of JK flipflop from T flipflop
2. Write short notes on SIPO and draw the output waveforms.
 | (15) | **BTL 6** | **Create** |

|  |  |  |
| --- | --- | --- |
| PRESENTSTATE | NEXT STATE | OUTPUT |
| x=0 | x=1 | x=0 | x=1 |
| a | f | b | 0 | 0 |
| b | d | c | 0 | 0 |
| c | f | e | 0 | 0 |
| d | g | a | 1 | 0 |
| e | d | c | 0 | 0 |
| f | f | b | 1 | 1 |
| g | g | h | 0 | 1 |
| h | g | a | 1 | 0 |

|  |
| --- |
| **UNIT IV - ASYNCHRONOUS SYNCHRONOUS SEQUENTIAL CIRCUITS AND****PROGRAMMABLE LOGIC DEVICES** |
| **Asynchronous sequential logic circuits- Transition tablity, flow tablility-race conditions, hazards & errors in digital circuits; analysis of asynchronous sequential logic circuits- introduction to Programmablility Logic Devices: PROM–PLA–PAL,CPLD-FPGA.** |
| **PART - A** |
| **Q.No** | **Questions** |  | **BT****Level** | **Competence** |
| 1. | Define racing |  | BTL-1 | Remember |
| 2. | What is critical race? |  | BTL-1 | Remember |
| 3. | What is meant by transition table? |  | BTL-1 | Remember |
| 4. | Estimate the types of hazards |  | BTL-5 | Evaluate |
| 5. | What is the difference between flow table and transition table? |  | BTL-4 | Analyze |
| 6. | Define races in Asynchronous sequential circuit. |  | BTL-1 | Remember |
| 7. | Predict the hazards in asynchronous sequential circuits? |  | BTL-2 | Understand |
| 8. | Show what is fundamental mode of operation in asynchronous sequential circuits? |  | BTL-3 | Apply |
| 9. | What is static hazard and dynamic hazard? |  | BTL-4 | Analyze |
| 10. | Define asynchronous sequential machine. |  | BTL-1 | Remember |
| 11. | Predict what is a PROM? |  | BTL-5 | Evaluate |
| 12. | State the difference between static 0 and static 1 hazard |  | BTL-2 | Understand |
| 13. | Compose about secondary variable and excitation variables. |  | BTL-6 | Create |
| 14. | Compare critical race and non critical race. |  | BTL-3 | Apply |
| 15. | What is flow table? Give example. |  | BTL-6 | Create |
| 16. | What is a deadlock condition? |  | BTL-1 | Remember |
| 17. | Deduce the demerits in designing asynchronous sequential machines. |  | BTL-2 | Understand |
| 18. | State the difference between PROM, PAL, PLA and EPROM. |  | BTL-3 | Apply |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 19. | What is a PLA? |  | BTL-2 | Understand |
| 20. | Point out the definition for flow table in asynchronous sequential circuit. |  | BTL-4 | Analyze |
| **PART B** |
| 1. | Design an asynchronous sequential circuit has two inputs X2 and X1 and one output Z. When X1=0, the output Z is 0. The first change in X2 that occurs while X1 is 1 will cause output Z to be 1. The output Z will remain 1 until X1 returns to 0. | (13) | BTL-6 | Create |
| 2. | 1. Implement the following function using PLA: F(x,y,z) = ∑m(1,2,4,6)
2. For the given Boolean function, obtain the hazard-free

circuit.F(A,B,C,D)=∑m(1,3,6,7,13,15) | (7)(6) | BTL-5 | Evaluate |
| 3. | 1. Obtain the PLA program table for a combinational circuit that squares a 3 bit number. Minimize the number of product terms.
2. A combinational circuit is defined by the functions. (a) F1(a,b,c)= ∑m(3,5,6,7)

(b) F2(a,b,c)= ∑m(0,2,4,5,7) | (7)(6) | BTL-1BTL-2 | RememberUnderstand |
| 4. | Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples. | (13) | BTL-4 | Analyze |
| 5. | Describe with reasons, the effect of races in asynchronous sequential circuit design. Explain its types with illustrations. Show the method of race-free state assignments with examples. | (13) | BTL-2 | Understan d |
| 6. | 1. Discover asynchronous BCD counter using JK flip- flops.
2. An asynchronous sequential circuit is described by Y=x1x’2+(x1 + x’2) y; z=y. Draw the logic diagram, transition table and output map.
 | (7)(6) | BTL-1BTL-4 | Remembe rAnalyze |
| 7. | 1. Find a circuit that has no static hazards and implement Boolean function

F(A,B,C,D)= ∑(0,2,6,7,8,10,12)1. Explain the different types of programmable logic devices with neat sketch and compare them.
 | (7)(6) | BTL-2BTL-4 | Understan dAnalyze |
| 8. | Derive the transition table and primitive flow table for thefunctional mode asynchronous sequential circuit shown in fig | (13) | BTL-2 | Understan d |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
| 9. | Implement the following function in PLA | (7) | BTL-3 | Apply |
|  | (i) F1=∑m(1,2,4,6); F2= ∑m(0,1,6,7); F3=∑m(2,6) |  |  |  |
|  | (ii) F1=∑m(3,5,8,9); F2= ∑m(2,3,5,8,); F3=∑m(0,1) | (6) |  |  |
| 10. | 1. Illustrate the following logic and analyse for the pressure of any hazard f=x1x2+x’1x3. If hazard is present briefly explain the type of hazard and design a hazard-free circuit.
2. Illustrate the following function in PLA f1(x,y,z) = ∑m(0,1,3,5,7)

f2(x,y,z) = ∑m(2,4,6) | (7) | BTL-4 | Analyze |
|  | (6) |  |  |
| 11. | Discover an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T=1& C moves from 1 to 0. Otherwise the output is 0. | (13) | BTL-1 | Remember |
| 12. | Discover an asynchronous BCD counter. | (13) | BTL-1 | Remember |
| 13. | Describe the steps involved in design of asynchronous sequential circuit in detail with an example. | (13) | BTL-3 | Apply |
| 14. | (i) How do you get output specifications | (4) | BTL-1 | Remember |
|  | from a flow table in asynchronous sequential |  |  |  |
|  | circuit operating in fundamental mode? |  |  |  |
|  | (ii) When do you get the critical and non- |  | BTL-1 | Remember |
|  | critical races? How will you obtain race free conditions? | (9) |  |  |
| **PART C** |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1. | (i) Design a PLA structure using AND and OR logic for the following function.F1=∑m(0,1,2,3,4,7,8,11,12,15) | (12) | BTL-6 | Create |
|  | F2=∑m(2,3,6,7,8,9,12,13) |  |  |  |
|  | F3=∑(1,3,7,8,11,12,15) |  |  |  |
|  | F4=∑(0,1,4,8,11,12,15) | (3) | BTL-2 |  |
|  | (ii) Compare PLA and PAL Circuits |  |  | Understand |
| 2. | A combinational circuit is defined by the functions F1=∑m(3,5,6,7) and F2=∑m(0,2,4,7). Implement the circuit with PLA and PAL design. | (15) | BTL-6 | Create |
| 3. | Design an asynchronous circuit that has two inputs x1 and x2 and one output z. the circuit is required to give an output whenever the input sequence (0,0),(0,1) and (1,1) received but only in that order. | (15) | BTL-6 | Create |
| 4. | An asynchronous sequential circuit is described by the | (4)(8)(3) | BTL-4 | Analyze |
|  | following excitation and the output function |  |  |
|  | Y=x1x2+(x1+x2)y. |  |  |
|  | (i) Draw the logic diagram of the circuit. |  |  |
|  | (ii) Derive the transition table and output map. |  |  |
|  | (iii) Describe the behaviour of the circuit. |  |  |

|  |
| --- |
| **UNIT V - VHDL** |
| **RTL Design –combinational logic –Sequential circuit –Operators –Introduction to Packages – Subprograms– Test bench. (Simulation/Tutorial Examples: adders, counters, flip flops, Multiplexers & De multiplexers).** |
|  | **PART - A** |
| **Q.No** | **Questions** |  | **BT** | **Competence** |
| 1. | What is a package in VHDL? |  | BTL-1 | Remember |
| 2. | Write the VHDL behavioural model for D-flip-flop. |  | BTL-1 | Remember |
| 3. | Write the VHDL code for a logical gate which gives high outputonly when both the inputs are high. |  | BTL-1 | Remember |
| 4. | Name any four hardware description language test benches. |  | BTL-1 | Remember |
| 5. | Give the syntax for package declaration and package body inVHDL |  | BTL-1 | Remember |
| 6. | Write VHDL code for 2\*1 MUX using behavioural modeling |  | BTL-1 | Remember |
| 7. | Deduce what is test bench? |  | BTL-4 | Analyze |
| 8. | Compose the operators used in VHDL |  | BTL-6 | Create |
| 9. | Compile VHDL code for half adder in data flow model. |  | BTL-6 | Create |
| 10. | Analyze the merits of hardware languages. |  | BTL-5 | Evaluate |
| 11. | What is the function of wait statement in VHDL package? |  | BTL-2 | Understand |
| 12. | Predict the need for VHDL. |  | BTL-4 | Analyze |
| 13. | Prepare the VHDL code for AND gate. |  | BTL-5 | Evaluate |
| 14. | Give the test bench for AND gate. |  | BTL-2 | Understand |
| 15. | Show the meaning of the following RTL statement? |  | BTL-3 | Apply |
| 16. | Categorize different test bench. |  | BTL-4 | Analyze |
| 17. | What is subprogram overloading? |  | BTL-2 | Understand |
| 18. | Expand the following acronyms. (a)VHDL (b)VHLSI |  | BTL-3 | Apply |
| 19. | What are the languages that are combined together to get VHDLlanguage? |  | BTL-3 | Apply |
| 20. | Write the VHDL code for full subtractor in data flow model. |  | BTL-2 | Understand |
|  | **PART - B** |
| 1. | Write the VHDL code to realize a full adder using (i) Behavioral modeling. (ii) Structural modeling. | (7+6) | BTL-1 | Remembe r |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 2. | Write the VHDL code to realize a 3-bit gray code counter using case statement. | (13) | BTL-1 | Remembe r |
| 3. | Write VHDL code for Binary UP/ DOWN counter using JK flip- flops. | (13) | BTL-1 | Remembe r |
| 4. | Design a 3 bit magnitude comparator and write the VHDL coding to realize it using structural modelling. | (13) | BTL-2 | Understan d |
| 5. | 1. Explain the digital system design flow sequence with the help of a flow chart.
2. Estimate a VHDL code for a 4 bit universal shift register.
 | (7)(6) | BTL-4BTL-4 | Analyze Analyze |
| 6. | Explain in detail the concept of Structural modelling in VHDLwith an example of full adder. | (13) | BTL-5 | Evaluate |
| 7. | 1. Explain in detail the various programming constructs used in VHDL for designing a logic circuit.
2. Discuss the various packages. Write a VHDL code for the implementation of decoder/de-multiplexer.
 | (7)(6) | BTL-4 BTL-4 | Analyze Analyze |
| 8. | (i) Write VHDL code for4 bit synchronous UP/DOWN counter and explain.ii) Write short notes on subprograms used for implementation of adders. | (8)(5) | BTL-1BTL-1 | RememberRemember |
| 9. | Design a VHDL code for full adder and 8\*1 MUX | (13) | BTL-6 | Create |
| 10. | Illustrate the VHDL code for JK master slave flip-flops and using JK FF as structural elements write code for 4 bit asynchronous counter. | (5+8) | BTL-4 | Analyze |
| 11. | Interpret the structural VHDL description for a 2 to 4 decoder in detail. | (13) | BTL-3 | Apply |
| 12. | Discover a VHDL code for 6 bit comparator and also explain the design procedure. | (13) | BTL-2 | Understan d |
| 13. | Discover a VHDL code for 4 bit binary counter with parallel load and explain. | (13) | BTL-2 | Understan d |
| 14. | 1. Explain the design procedure of RTL using VHDL.
2. Write a note on VHDL test benches.
 | (8)(5) | BTL-3BTL-3 | ApplyApply |
| **PART - C** |
| 1. | Design a 4 X 4 array multiplier and write the VHDL coding to realize it using structural modelling. | (15) | BTL-6 | Create |
| 2. | 1. Discover the VHDL code for 3 to 8 decoder.
2. Discover the VHDL code for 4:1 multiplexer.
 | (8)(7) | BTL-6 | Create |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 3. | 1. Discuss briefly the packages in VHDL
2. Write an VHDL coding for realization of clocked S-R flip

flop. | (7)(8) | BTL-5 | Evaluate |
| 4. | i) Write short notes on built-in operators used in VHDL | (7) | BTL-3 | Apply |
|  | programming. |  |  |  |
|  | ii) Write VHDL coding for 4 X 1 Multiplexer | (8) |  |  |