EC6601 VLSI DESIGN

UNIT I: MOS TRANSISTOR PRINCIPLE
PART A-C312.1

1. What are the advantages of SiO_2 as a dielectric?

SiO_2 has a relatively low loss & high dielectric strength, thus application of high gate fields is possible.

2. State the 3 modes involved in the operation of an enhancement transistor

1. Accumulation mode 2.Depletion mode 3. Inversion mode.

3. What are the factors that influence the drain current?

The distance between source and drain
The channel width
The threshold voltage V_t
The thickness of the gate – insulating oxide layer
The dielectric constant of the gate insulator
The carrier (electron or hole) mobility, μ.

4. Compare CMOS and Bipolar technologies. (Nov/Dec 2013)

S.No.	CMOS Technology	Bipolar Technology
1.	Low static power dissipation	High power dissipation
2.	High input impedance	Low input impedance
3.	High packing density	Low packing density
4.	Low output drive current	High output drive current
5.	Drain and source are interchangeable	It is unidirectional
6.	High noise margin	Low voltage swing logic

5. Define threshold voltage and state the parameters on which it is dependent on.

Vt can be defined as the voltage applied between gate & source of an MOS device below which Ids effectively drops to zero. It is a function of

- Gate conductor material
- Gate insulation material
- Gate insulator thickness - channel doping
- Impurities at the silicon insulator interface
- Voltage between the source and the substrate,Vsb.

6. Define Body effect. (Nov/Dec 2016)

The threshold voltage Vt is not constant with respect to the voltage difference between the substrate and the source of the MOS transistor.

So, when several MOS devices are connected in series, the threshold voltage is increased due to voltage difference between the substrate and the source. This effect of body or substrate voltage is called body effect.

7. State channel length modulation? Write down the equation for describing the channel length modulation effect in NMOS transistors. (May/June 2016), (April / May 2017)

When an MOS device is in saturation, the effective channel length is decreased such that, $L_{eff} = L - L_{short}$. Where $L_{short} = \sqrt{2(\varepsilon_{si}/qNa)(Vds - (Vgs - Vt))}$

The reduction in channel length increases the W/L ratio, thereby increasing β as the drain voltage increases.

8. Define rise time(t_r).

Rise time(t_r) is the time for a waveform to rise from 10% to 90% of its steady state value.

9. Define noise margin (May/June 2014). Illustrate how it can be obtained from the transfer characteristics of a CMOS Inverter. (Nov/Dec 2016)

Noise margin is a parameter that allows us to determine the allowable noise voltage on the input of a gate so that the output will not be affected. The 2 common parameters are N_{MH} & N_{ML} Where

$N_{ML} = |V_{ILmax} - V_{OLmax}|$ and $N_{MH} = |V_{OHmin} - V_{IHmin}|$

V_{IHmin}=minimum HIGH input voltage
V_{ILmax} = maximum LOW i/p voltage
V_{OHmin} = minimum HIGH o/p voltage
V_{OLmax} = maximum LOW o/p voltage

10. Define fall time (t_f)

Time for a waveform to fall from 90% to 10% of its steady state value.

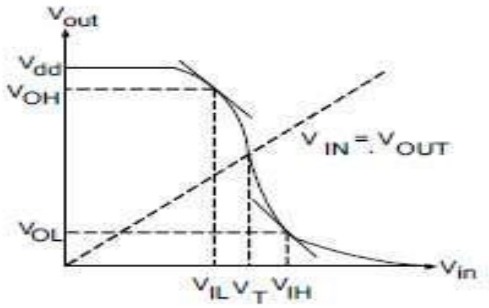
11. Define delay time,t_d.

Time difference between input transition and 50% output level .This is the time taken for a logic transition to pass from input to output.

12. Discuss any two layout design rules? (May/June 2014)

The two main approaches for describing layout rules are (i) micron rule (ii) μ- based rules. Micron design rules give a list of minimum feature sizes and spacing for all the masks required in a given process. λ-based design rules are based on a single parameter, 'λ' which characterizes the linear feature- the resolution of the complete wafer implementation process

13. Draw the DC transfer characteristics of CMOS inverter? (Nov/Dec 2013), (April/May 2015)



V_{IH}: minimum HIGH input voltage, V_{IL}: maximum LOW input voltage, V_{OH}: minimum HIGH output voltage, V_{OL}: maximum LOW output voltage. V_T – Threshold voltage

14. What are the advantages of twin tub process? Used for protection against latch-up.

Provides separate optimization of p-type & n-type transistors

15. What is BiCMOS?

BiCMOS is the combination of bipolar & CMOS transistors.

To reduce the delay times of the highly loaded signals (microprocessor busses) and to provide better performance for analog functions the bipolar devices (npn or pnp) can be added to MOS transistors or vice versa.

16. What are the advantages of SOI process?

- There is no latch-up.
- There are no body-effect problems
- No field-inversion problems

Lower substrate capacitances provide the possibility for faster cirecuits.

17. What is the objective of the layout rules? (Nov ')2012

To obtain a circuit with optimum yield in as small an area as possible without compromising reliability of the circuit.

18. What are the types of layout design rules? Micron rule, Lambda based rule.

19. What is passivation or overglass?

This is a protective glass layer that covers the final chip. Openings are required at pads and any internal test points.

20. What are the types of oxidation?

- Wet Oxidation: The oxidizing atmosphere contains water vapour
- Dry Oxidation: The oxidizing atmosphere is pure oxygen

21. What are the advantages of EBL pattern generation?

- Patterns are derived directly from digital data
- There are no intermediate hardware images
- Different patterns may be accommodated in different sections of the wafer without difficulty.
- Changes to patterns can be implemented quickly.

22. What are the types of etching process?

Isotrophic etch, fully anisotrophic etch, Preferential etch.

23. What is a thinox?

Thinox is an active mask formed which defines the areas where thin oxide are needed to implement transistor gates and allow implantation to form P or N-type diffusions for transistor source/drain regions.

24. What are the non –ideal I-V effects? (May/June 2014)

Velocity Saturation, Channel Length Modulation, Body Effect, Leakage and Temperature Sensitivity

25. Define scaling? (Nov/Dec 2013), (April/May 2015)

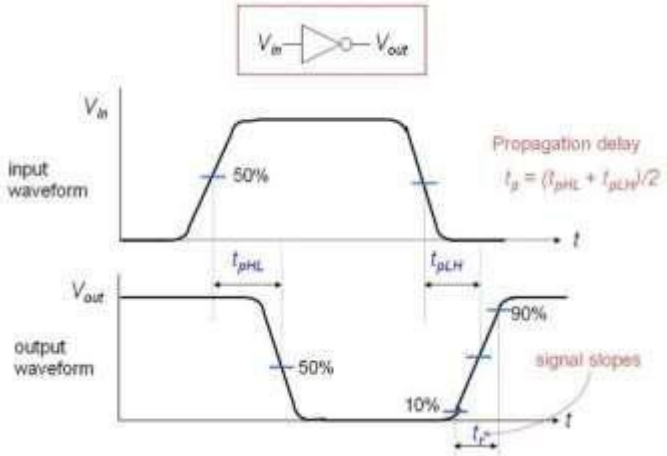
Scaling of MOS transistor is concerned with systematic reduction of overall dimensions of the devices as allowed by the available technology, while preserving the geometric ratios found in the larger devices.

26. What is contamination delay time t_{cd}?

It is the minimum time from the input crossing 50% to the output crossing 50%.

27. What is propagation delay time t_{pd}? / Define propagation delay of a CMOS inverter. (May/June 2014), (May/June 2016), (April / May 2017)

It is the maximum time from the input crossing 50% to the output crossing 50%. It is also called as Max-time.



High-to-Low propagation delay (t_{pHL}): Time taken to fall from V_{OH} to 50%.
Low-to-High propagation delay (t_{pLH}): Time taken to rise from 50% to V_{OL}.
Propagation Delay (t_p): (t_{pHL} + t_{pLH})/2.

28. Give the types of scaling in CMOS technology. (Nov/Dec 2013) Transistor scaling, Interconnect scaling

29. What is a stick diagram? (Nov/Dec 2014)

Stick diagrams are commonly used to represent the topology of CMOS integrated circuits. With a little annotation (FET width and length) they provide adequate information to guide layout and mask generation.

30. Define lambda based design rules used for layout. (April/May 2015)

λ- based design rules are based on a single parameter, 'λ' which characterizes the linear feature- the resolution of the complete wafer implementation process.

31. What do you mean by design margin?(May/June 2014)

Design Margin required as there are three sources of variation- two environmental and one Manufacturing which are given as below, Supply Voltage, Operating temperature Process variation

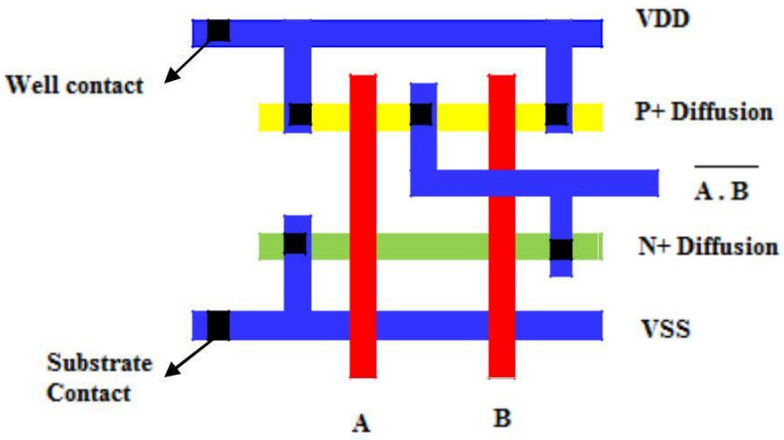
32. What is threshold voltage?

The threshold voltage is defined as the values of V_{gs} below which I_{ds} becomes zero. In the real transistor characteristics, sub-threshold current continues to flow for $V_{gs} < I_{ds}$. The threshold voltage varies with L,W, V_{ds} and V_{bs} .

33. What is latch-up? How to prevent latch-up? (May/June 2016)

Latch-up is the shorting of the VDD & VSS lines in CMOS fabrication process due to parasitic circuit effect. Latch-up results in chip self-destruction or system failure. Latch-up can be prevented by using Latch-up resistant CMOS process and Layout techniques.

34. Sketch the layout of a 2-input NAND gate. (NOV/DEC 2016)



PART B-C312.1

1. (a) Explain the operation of a CMOS inverter clearly indicating the various regions of operation.(12)
   (b) List the advantages of Lambda based design rules as compared to micron based design rules.(4)

2. (a).Discuss the aspects of MOS transistor threshold voltage.(8)
   (b) Derive the VTC of CMOS inverter. (8)
3. (a). Discuss the operation of CMOS inverter with diagrams.(8)
   (b) Discuss the mead Conway design rules for the silicon gate NMOS process. (8)
4. Explain in detail about the ideal I-V characteristics and non ideal I-V characteristics of NMOS and PMOS devices and derive its equation.**(May/June 2013) (May/June 2016) (Nov/Dec 2016)**
5. (i) Draw and explain the n-well process (10)
   (ii) Explain the twin tub process with a neat diagram (6)
6. (i) Discuss the origin of latch up problems in CMOS circuits with necessary diagrams. Explain the remedial measures. (10)
   (ii) Explain the electrical properties of MOS transistor in detail **(Nov/Dec 2013)**
7. Briefly discuss about the CMOS process enhancements and layout design rules. **(May/June 2014)**
8. Discuss the steps involved in IC fabrication process (16)
9. Describe n- well process in detail (16) **(Nov/Dec 2016)**
10. Explain with neat diagrams the SOI process and mention its advantages**.(Nov'2012)**
11. Discuss the CV characteristics and DC transfer characteristics of the CMOS. **(May/June2014)**
12. Explain the various steps involved in the P-well CMOS process with necessary diagrams **(Nov'2012)**
13. Explain in detail about the scaling concept of CMOS chips. **(May/June2013)**
14. Explain in detail about Device models. **(May/June 2014)**
15. (i) Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics. **(May/June 2016)**
    (ii) Explain in detail about the body effect and its effect in NMOS and PMOS devices **(May/June 2013) (May/June 2016)**
16. (i) Explain the DC characteristic of a CMOS inverter with necessary conditions for the different regions of operation **(Nov'2013), (May/June 2016)**
    (ii)Discuss the principles of constant field and lateral scaling. Write the effects of the above scaling methods on device characteristics. **(May/June 2016)**
    (ii) Draw the layout diagram for NAND and NOR gate.
17. Explain the need for scaling principles and fundamentals units of CMOS inverter.
18. (i) Draw and explain the DC and transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation.
    (ii) Draw the layout diagram of NAND and NOR gate. **(May/June 2017)**

UNIT II: COMBINATIONAL LOGIC CIRCUITS
PART A- C312.2

1.What are critical paths?

Critical paths are logic paths that require attention to timing details. Designers use a timing analyzer to find the slowest path in a logic design. Quick delay estimation is essential to design critical paths.

2.List the levels affecting critical path.

The architectural / micro architectural level, the logical level, the circuit level, and the layout level.

3.What are the depending factors for delay of a logic gate?

- Width of the transistors in the gate.
- Capacitance of the load that must be driven.

4. How do you determine gate and diffusion capacitance?

Gate capacitance can be determined from the transistor width form the schematic and diffusion capacitance depends on the layout.

5. **Give the equation for elmore delay model**./ **Define Elmore constant. (April / May 2017)**

$$t_{pd} = \sum R_{n-i}\, C_i = \sum_{i=1}^{N} C_i \sum_{j=1}^{N} R_j$$

where N is the total number of nodes in the RC equivalent circuit, R_{n-i} is the resistance of the portion of the path to the capacitance C_i, R_j is the resistance at node j and C_i is the capacitance at node i.

R_{n-i} = Node in the ladder of resistance R_{n-i} between the node and a supply.

6. Define logical effort.

Logical effort is defined as the ratio of input capacitance of the gate to that of the input capacitance of an inverter that can deliver the same output current. It is independent on the size. It helps to estimate the delay

of the entire path quickly based on the parasitic and logical delay of the path.

7. What is electrical effort?

It is the ratio of load capacitance to input capacitance. It is also called as the fan-out. This depends on the size.

8.What is parasitic delay?

The parasitic delay of the gate is the delay of the gate when it drives zero load. It can be estimated with RC delay models.

9.Give the equations that express the delay of a logic gate.

d= f + p , p=> Parasitic delay, f => Effort delay/ Stagg effort f

= g.h , g => Logical effort , h=> electrical effort/Fan-out

$h=C_{out} / C_{in}$; C_{out} => Capacitance of the external load being driven.

C_{in}=> Input capacitance of the gate.

10.What is path delay?

It is the sum of delays of each stage. It is the sum of the path effort delay D_f and path parasitic delay

P. $D= \Sigma di = D_f + P$, where $D_f = \Sigma fi$ & $P= \Sigma Pi$

D_f – Path Effort delay, di-delay of a gate i,P-parasitic delay, fi –Effort delay at gate i and Pi is the parasitic delay at gate i

11.Give the factors that give rise to static power dissipation.(Nov/Dec 2013)

Sub-threshold conduction through off transistors. Tunneling the current through gate oxide. Leakage through reverse biased diodes. Contention current in the ratioed circuits.

12.Give the factors that produce dynamic power dissipation.(Nov/Dec 2013)

- Charging and discharging of load capacitance.
- Short term current when both PMOS and NMOS networks are partially ON .

13.Give the formula for static power dissipation

$P_{static} = T_{static} V_{DD}$

14.Write the formula for dynamic power dissipation.

$P_{dynamic}=C V_{DD}^2 f_{sw}$

C=> Load capacitance

V_{DD}=> High potential / power

f_{sw} => average frequency

15. How do we reduce dynamic power?

Activity for reduction, Reduction of the inter connect switching capacitance and Choose lower power supply /operating frequency.

16. State the types of power dissipation. (April/May 2015)

- Static power dissipation
- Dynamic power dissipation

17. What is a transmission gate?

A transmission gate consists of an n- channel transistor and a p – channel transistor with separate gate connections and common source and drain connections. It gives good transmission of both logic 1 and logic 0.

18. Define Transistor Sizing problem. (May/ June 2014)

Transistor sizing, an important problem in designing high performance circuits, has traditionally been formally defined as

Minimize *Area* or *Power*

Subject to *Delay _ Tspec*:

19. What does the two letters in units denote in SPICE?

The first character indicates the order of magnitude and the second letter indicates a unit for human convenience and is ignored by SPICE.

20. Why is the transmission of logic 1 degraded as it passes through a nmos pass transistor. (Nov/Dec 2016)

When S = 1 (Vdd) , and Vin = 1 the pass transistor begins to conduct and charges the CL towards Vdd.Initially Vin is at ahigher potential than Vout, the current flows through the device. As voltage ot the load approaches Vdd – Vtn, the n- device begins to turn – off. Vtn is the n- transistor body effected threshold .. Thus the transmission of logic 1 is degraded.

21. List the various power losses in CMOS circuits? (May/June 2013)

22. Write the equation for total static power dissipation.

$Ps = \sum$ leakage current X supply voltage ; 1

n = no: of devices

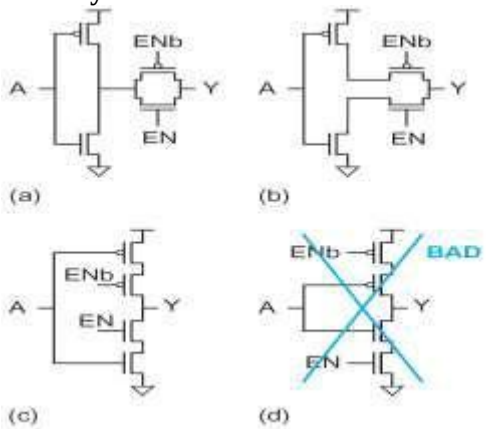
23. What is a pass transistor? What are its advantages? (Nov 2013) Pass transistor is similar to a buffer.

Advantages of pass transistor are

i .Occupies less space, because any logical operation can be realized with lesser number of MOS transistors

ii. No direct path between VDD and Gnd. So, amount of power dissipation is lesser understand by condition.

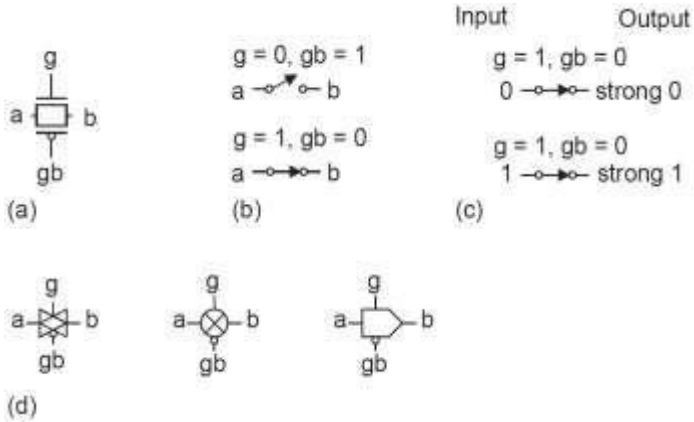
24. Draw the structure & symbol of a CMOS tri - state inverter.



25. What are the disadvantages of CMOS transmission gates? Draw the symbol for transmission gate.

Disadvantages of CMOS transmission gate are, Require more area than NMOS pass circuits Require complemented control signals

T.G symbol



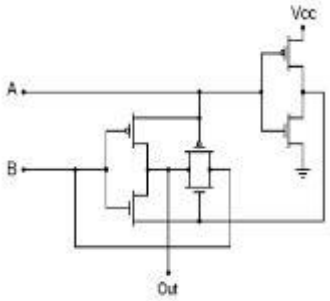
26. What is meant by domino logic ?

Domino logic module consists of a PE logic block followed by an Inverter. This ensures that all inputs to the next logic block are set to 0 after the precharge period. So, only the possible transition during the evaluation period is the 0-1 transition.

27. List the disadvantages of dynamic logic.

(i) Logic function is implemented by the NMOS pull down network.
(ii) Less no. of transistors required.
(iii) Noise margin doesn't depend on transistor ratios
(iv) Consumes only dynamic power.
(v) Faster switching speeds.

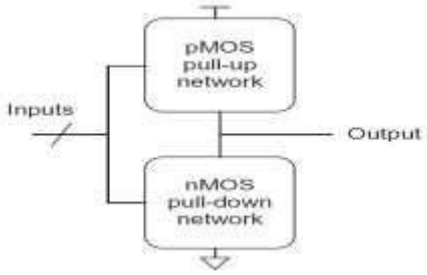
28. What is a transmission gate? Realize a 2-input XOR gate using transmission gates.



A transmission gate consists of an n- channel transistor and a p – channel transistor with separate gate connections and common source and drain connections. It gives good transmission of both logic 1 and logic 0.

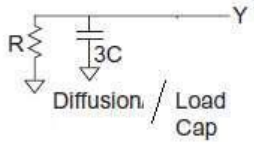
29. What is a pull – down device?

A pull-up device when energized will pull the ouput to supply(i.e "1") and a pull-down will pull the output to ground (i.e. "0"). Usually PMOS is used for pull-up since it can provide "1" (HIGH) i.e VDD and NMOS is pull-down since it can provide a "0" i.e. (LOW).



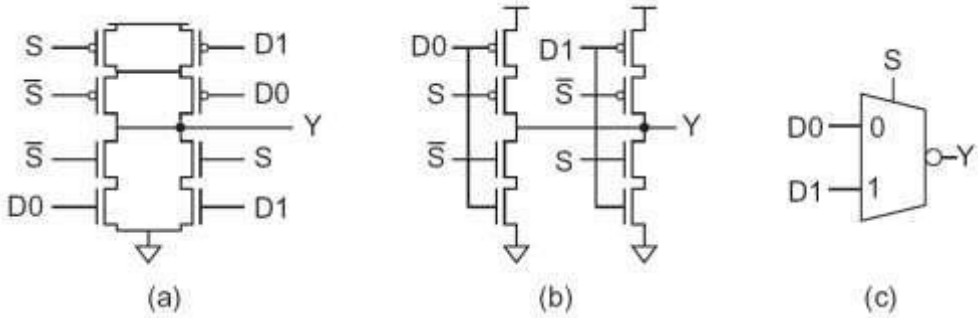
30. State any two criteria for low power logic design? (Nov/Dec 2013) Supply voltage transistor sizing and clock gating

31. Give Elmore delay expression for propagation delay of an inverter. (May/June 2016) Equivalent circuit of an inverter for the falling transition:

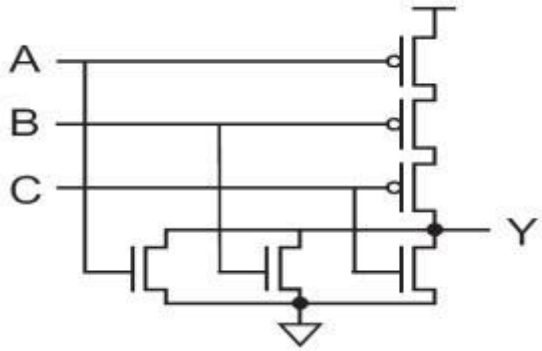


$t_{pdf} = t_{pdr} = 3RC$

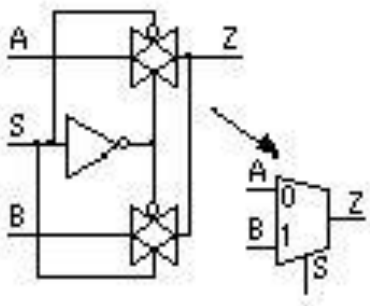
32. Draw the structure of 2:1 CMOS MUX.(Nov/Dec 2013)



33. Draw the switch logic arrangement for CMOS 3-input NOR gate.



34. Draw 2-input MUX gate using transmission gates.



35. Why single phase dynamic logic structure cannot be cascaded? Justify. (May/June 2016)

Single phase dynamic logic structure cannot be cascaded. Because, a fundamental difficulty with dynamic circuits is the monotonicity requirement. While a dynamic gate is in evaluation, the inputs must be monotonically rising. Unfortunately, the output of a dynamic gate begins HIGH and monotonically falls LOW during evaluation. This monotonically falling output X is not a suitable input to a second dynamic gate expecting monotonically rising signals, as shown in Figure. Dynamic gates sharing the same clock cannot be directly connected. This problem is often overcome with domino logic.

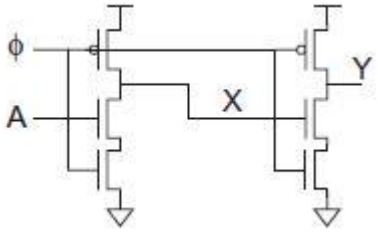


Figure: Incorrect connection of dynamic gate 36. State the advantages of transmission gates. (April / May 2017)

The NMOS only pass transistor can only pass strong zero at the output where as it cannot pass strong one. Similarly, PMOS only pass transistor can only pass strong one at the output where as it cannot pass strong zero. The disadvantages of both PMOS and NMOS pass transistor is overcome by transmission gate where it is able to produce both strong one and strong zero at the output.

37. List out the sources of static and dynamic power consumption.(Nov/Dec 2016)

CMOS devices have very low static power consumption, which is the result of leakage current. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

PART B- C312.2

1. Discuss in detail about the various delay models in CMOS technology.
2. What is meant by power dissipation? Derive an expression for static power dissipation and dynamic power dissipation with necessary diagram and expressions. **(Nov/Dec 2013) / (May/June 2014) (Nov/Dec 2016)**
3. Explain low power design.
4. Explain the resistive and capacitive delay estimation of CMOS inverter circuit **(May/June2013)**
5. Find the rising and falling propagation delays of an AND- OR- INVERT gate using the Elmore delay model (**Nov/Dec 2013)**
6. Draw a 3- input NAND gate with its gate and diffusion capacitance. Assume all diffusion nodes are contacted.
7. What is a pass transistor? What are their limitations? Why? Explain how transmission gates are built and their principle of operation. (16)
8. Construct a 8 to 1 multiplexer using CMOS devices. Give necessary explanation. (8)
9. Explain why the transmission gate of logic 1 is degraded as it passed through an MOS pass transistor
10. Design NAND gate using pseudo –nMOS Logic. **(Nov/Dec 2013)**
11. Implement the following function using CMOS
    f(A,B,C) = A'BC + AB'C + ABC' (8)
    y= (A+B)(C+D) (8) **(Nov/Dec 2013)**
12. Describe the different methods of reducing static and dynamic Power dissipation in CMOS circuits **(May/June 2013)**
13. Explain the domino and dual rail domino logic families with neat diagrams**.(Nov'2012)**
14. Write a brief note on sequencing dynamic circuits **(Nov'2012)**
15. Briefly discuss about the classification of circuit families and comparison of circuit families **(May/June 2014)**
16. (i) Draw the static CMOS logic circuit for the following expression
    (a) Y=(A.B.C.D)' (b) Y=(D(A+BC))'
    (ii) Discuss in detail about the characteristics of transmission gate. **(May/June 2016)**
17. What are the sources of power dissipation in CMOS and discuss various design technique to reduce power dissipation in CMOS? **(May/June 2016)**
18. (i) Explain about DCVSL logic with suitable example.
    (ii) What is transmission gate? Explain the use of transmission gate. **(April / May 2017)**
19. Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams

and expressions. **(April / May 2017)**

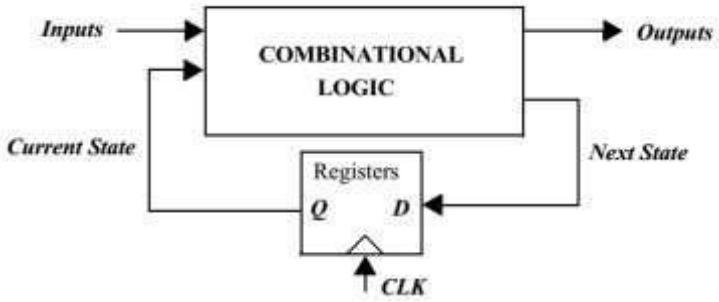
20.Write short notes on i) Ratioed circuits ii) Dynamic CMOS circuits. **(Nov/Dec 2016)**

UNIT III: SEQUENTIAL LOGIC CIRCUITS
PART A- C312.3

1. Differentiate combinational and sequential logic circuits.

Combinational logic circuits have the property that the output of a logic block is only a function of the current input values, assuming that enough time has elapsed for the logic gates to settle. In sequential logic circuits, the output depends not only on the current values of the input, but also on preceding input values- i.e., they have memory.

2. Draw the block diagram of a Finite State Machine



3. List the timing metrics for sequential circuits.

The three important timing parameters associated with a register are : setup time, hold time and propagation delay.

4. What is the importance of setup time, hold time and propagation delay associated with a register?

Setup time is the time the data inputs must be valid before the clock transition. The hold time is the time the data input must remain valid after the clock edge. Assuming that the setup and hold times are met, the data at the input is copied to the output after a worst case propagation delay, with reference to the clock edge.

5. How can memory elements be classified?

Memory elements be classified as:

- Foreground vs Background Memory
- Static vs Dynamic Memory
- Latches vs Registers

6. How is a latch different from a register? (Nov/Dec 2014)

A latch is level sensitive circuit that passes the D input to the Q output when the clock signal is high. Contrary to level sensitive latches, edge triggered registers only sample the input on a clock transition, that is $0 \rightarrow 1$ for a positive edge triggered register and $1 \rightarrow 0$ for a negative edge triggered register.

7. What is a flip-flop?

A flip flop is any bistable element formed by cross coupling of gates. A flip flop is useful only if there exists a means to bring it from one state to the other.

8. What is meant by clock skew?

Variations can exist in the wires used to route two clock signals, or the load capacitance can vary based on data stored in the connecting latches. This effect, known as clock skew, is a major problem, causing the two clock signals to overlap.

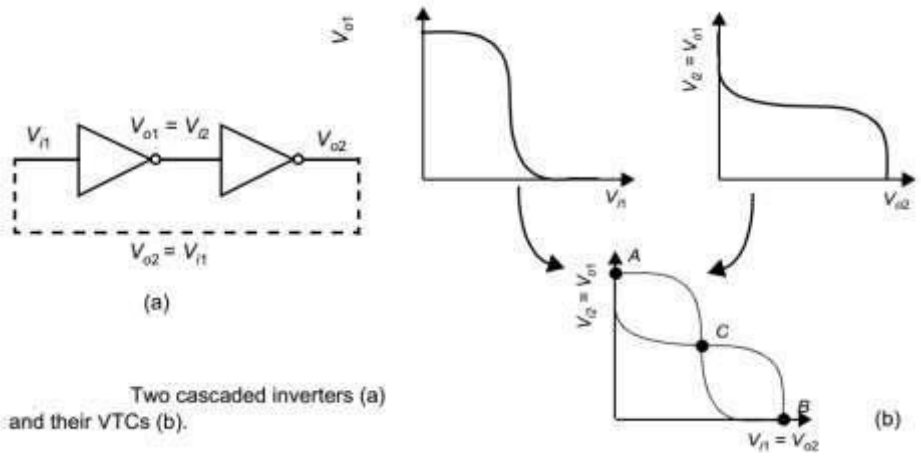
9. What is the major disadvantage of a static gate?

The major disadvantage of the static gate, however, is its complexity. When registers are used in computational structures that are constantly clocked such as pipelined datapath, the requirement that the memory should hold state for extended periods of time can be significantly relaxed. This results in a class of circuits based on temporary storage of charge on parasitic capacitors. The principle is exactly identical to the one used in dynamic logic — charge stored on a capacitor can be used to represent a logic signal. The absence of charge denotes a 0, while its presence stands for a stored 1. No capacitor is ideal, unfortunately, and some charge leakage is always present. A stored value can hence only be kept for a limited amount of time, typically in the range of milliseconds. If one wants to preserve signal integrity, a periodic *refresh* of its value is necessary. Hence the name *dynamic* storage.

10. What is the advantage of dual-edge triggered registers?

It is also possible to design sequential circuits that sample the input on both edges (rising or falling). The advantage of this scheme is that a lower frequency clock (half of the original rate) is distributed for the same functional throughput, resulting in power savings in the clock distribution network.

11. Draw the Voltage Transfer Characteristics of two cascaded inverters.



Two cascaded inverters (a) and their VTCs (b).

12. What are the timing parameters for electronic memories?

- The time it takes to retrieve data from memory is called the read access time, which is equal to the time between the read request and the moment the data is available at the input**.**
- The write access time is the time elapsed between a write request and the final writing of the input data to the memory.
- Cycle time is the minimum time required between successive reads or writes.

13. List the memory classification based on memory functionality.

A distinction is made between read-only (ROM) and read- write (RWM)memories.

RWM memories offer both read and write functionality with comparable access times. They may be either static or dynamic. They belong to the class of volatile memories.

ROM encodes the information into the circuit topology, for example, by adding or removing transistors. Since this topology is hard wired, the data cannot be modified. They belong to the class of non volatile memories.There are also non volatile read write memories (NVRWM). Members of this family are EPROM,E2PROM and flash memories.

14. How can memories be classified based on access pattern?

Most memories belong to the random access class, which means memory locations can be read or written in a random order. Some memory types restrict the order of access, which results in either faster access times, smaller area or a memory with special functionality. Examples of such are the serial memories: FIFO,LIFO and shift register. Video memories and CAM also belong to this class.

15. What is the peculiarity of a CAM?

Content addressable memories represent an important class of non random access memories. Instead of using an address to locate the data, a CAM uses a word of data itself as input in a query style format. When the input data matches a data word stored in the memory array, a MATCH flag is raised. The MATCH signal remains low if no data stored in the memory corresponds to the input word. They are an important component of cache architecture of many microprocessors.

16. List the advantages of two phase clocking scheme.(Nov '04)

(i) No chance of race conditions occurring in the circuit
(ii) No timing errors due to races or Hazards or clock skew
(iii) Two phase clocking schemes are popular due to its simplicity & reliability
(iv) Design procedures are also simple

17. What is the advantage of using a block address in memory design?

- The length of the local word and bit lines-that is the length of the lines within the blocks- is kept within bounds, resulting in faster access times.
- The block address can be used to activate only the addressed block. Non active blocks are put in a power saving mode with sense amplifiers and row and column decoders disabled. This results in a substantial power saving.

18. What is meant by a 'synchronous' approach to system design?

All sequential circuits have one property in common—a well-defined ordering of the switching events must be imposed if the circuit is to operate correctly. If this were not the case, wrong data might be written into the memory elements, resulting in a functional failure. The *synchronous* system approach, in which all memory elements in the system are simultaneously updated using a globally distributed periodic synchronization signal (that is, a global clock signal), represents an effective and popular way to enforce this ordering. Functionality is ensured by imposing some strict contraints on the generation of the clock signals and their distribution to the memory elements distributed

over the chip; non-compliance often leads to malfunction.

19. List the timing classification of digital systems.

In digital systems, signals can be classified depending on how they are related to a local clock.Signals that transition only at predetermined periods in time can be classified as synchronous, mesochronous, or plesiochronous with respect to a system clock. A signal that can transition at arbitrary times is considered asynchronous.

Synchronous Interconnect: A synchronous signal is one that has the exact same frequency, and a known fixed phase offset with respect to the local clock. In such a timing methodology, the signal is "synchronized" with the clock, and the data can be sampled directly without any uncertainty.

Mesochronous interconnect :A mesochronous signal is one that has the same frequency but an unknown phase offset with respect to the local clock ("meso" from Greek is middle). For example, if data is being passed between two different clock domains, then the data signal transmitted fromthe first module can have an unknown phase relationship to the clock of the receiving module. In such a system, it is not possible to directly sample the output at the receivingmodule because of the uncertainty in the phase offset.

Plesiochronous Interconnect A plesiochronous signal is one that has nominally the same, but slightly different frequency as the local clock ("plesio" from Greek is near). In effect, the phase differencedrifts in time. This scenario can easily arise when two interacting modules have independent clocks generated from separate crystal oscillator.

Asynchronous Interconnect: Asynchronous signals can transition at any arbitrary time, and are not slaved to any local clock. As a result, it is not straightforward to map these arbitrary transitions into a synchronized data stream.

20. What is meant by clock jitter?

Clock jitter refers to the temporal variation of the clock period at a given point — that is, the clock period can reduce or expand on a cycle-by-cycle basis. It is strictly a temporal uncertainty measure and is often specified at a given point on the chip. Jitter can be measured and cited in one of many ways. *Cycle-to-cycle jitter* refers to time varying deviation of a single clock period and for a given spatial location *i* is given as $T_{jitter,i}(n) = T_{i, n+1} - T_{i,n} - T_{CLK}$, where $T_{i,n}$ is the clock period for period *n*, $T_{i, n+1}$ is clock period for period $n+1$, and T_{CLK} is the nominal clock period.

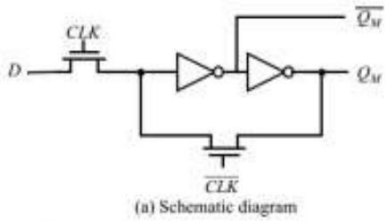
21. Is D-flip-flop applicable for counter applications? Why?

D-latch is not an edge triggered storage element because the output changes according to the input, ie, latch is transparent, when the clock is high. Due to this transparency property, it is unsuitable for counter applications.

22. What are synchronizers? (May/June 2014, May/June 2013)

Synchronizers are a necessity to protect us from their fatal effects. Originally, synchronizers were required when reading an asynchronous input (that is, an input not synchronized with the clock so that it might change exactly when sampled). Now, with multiple clock domains on the same chip, synchronizers are required when on-chip data crosses the clock domain boundaries.

23. Draw the switch level schematic of multiplexer based nMOS latch using nMOS only pass transistors for multiplexers. (May/June 2016)



(a) Schematic diagram

Multiplexer-based NMOS latch using NMOS-only pass transistors.

24. What is clocked CMOS Register? (May/June 2016)

The C^2MOS Register

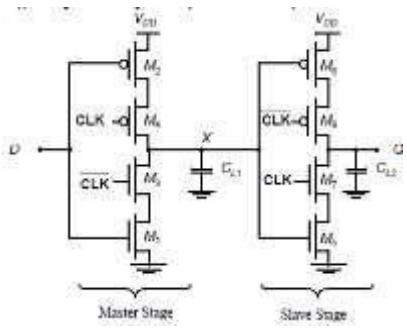


Figure shows an ingenious *positive edge-triggered* register, based on a *master-slave* concept insensitive to clock overlap. This circuit is called the C^2MOS (Clocked CMOS) *register.*

The overall circuit operates as a *positive edge-triggered master-slave* register —very similar to the transmission-gate based register. However, there is an important difference: A C^2MOS register with *CLK-CLK'* clocking is insensitive to overlap, as long as the rise and fall times of the clock edges are sufficiently small.

25. What is meant by pipelining? (April / May 2017)

Pipelining allows different functional units of a system to run concurrently. Pipelining cannot decrease the processing time required for a single task. The advantage of pipelining is that it increases the throughput of the system when processing a stream of tasks.

26. Compare and contrast synchronous design and asynchronous design. (April / May 2017)

Asynchronous design	Synchronous Design
Clock pulse is given to first circuit and the output of first circuit acts as a clock to the next and so on.	Simultaneous clock pulse is given to all the circuits.
Slow as compare to synchronous circuits	Fast as compare to asynchronous circuits.
Circuit is simple as compared to synchronous circuits.	Additional combinational circuit is required for its designing. This circuit becomes complex.

PART B- C312.3

1. Highlight the difference between combinational and sequential logic circuits. Draw and explain the block diagram of a Finite State Machine.
2. Explain the timing metrics for sequential circuits with neat diagrams.
3. Briefly explain the difference between Static and Dynamic Memory
4. Elaborate on the differences between latches and registers with necessary timing diagrams. **(Nov/Dec 2016)**
5. Explain the Bistability Principle associated with static latches and registers.
6. How can we build latches using multiplexers? Explain their operation in detail.
7. What is the common approach for constructing an edge triggered register? Hence explain the operation of a register based on master-slave configuration.
8. What is the drawback of transmission gate register? What is the approach to overcome it?
9. (i) What kinds of failures are caused by clock overlap? What is race condition?
   (ii) What approach is adopted to overcome the above? Explain with neat schematics.
10. Explain the operation of Static SR flip flops built using NOR and NAND gates.
11. Explain the operation of a Dynamic Transmission Gate Edge Triggered Register.
12. How can one design a register that is insensitive to clock-skew?
13. Explain the concept of pipelining in connection with sequential circuit optimization.
14. Explain the NORA-CMOS logic style for pipelined structures. Is this topology race free? **(Nov/Dec 2016)**
15. Illustrate various clocking strategies used in chip design.
16. Describe the architecture of an N-word memory.
17. Explain the organization of a memory array.
18. Briefly explain the operation of various memory peripheral circuitries.
19. What are the different approaches to reduce power dissipation in memories?
20. Discuss the impact of clock skew and jitter on the performance of a sequential system.
21. Characterize in detail the various sources of skew and jitter.
22. Explain different clock distribution schemes.
23. What are the challenges involved in an asynchronous design? Can these challenges be overcome using a self-timed logic?
24. Explain the concept and implementation of synchronizers and arbiters.
25. Illustrate the basic concept of clock synthesis and synchronization using Phase –Locked loop.
26. Compare synchronous and asynchronous design.
27. Explain the methodology of sequential circuit design of latches and flip-flops **(May/June 2014)**
28. Discuss the operation of a pipeline concepts used in sequential circuits **(May/June 2013)**
29. Write a brief note on sequencing dynamic circuits **(Nov'2012)**
30. (i) Design D-flip-flop using transmission gate. **(Nov/Dec 2013)**
    (ii) Implement a 2- bit non-inverting dynamic shift register using pass transistor logic.

31. Explain the operation of master slave based edge triggered register**(May/June 2016)**

32. Discuss in detail about various pipelining approaches to optimise sequential circuits**(May/June 2016)**

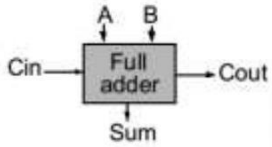
33. (a)Explain the operation of true single phase clocked register
(b)Draw and explain the operation of conventional ,pulsed and resettable latches**(APRIL/MAY 2017)**

34. Explain the concept of timing issue and pipelining**(APRIL/MAY 2017)**

UNIT IV- DESIGNING ARITHMETIC BUILDING BLOCKS

PART A- C312.4

1.Draw the truth table of a binary full adder and write the expressions for sum and carry output.



A	B	C_i	S	C_o	Carry status
0	0	0	0	0	delete
0	0	1	1	0	delete
0	1	0	1	0	propagate
0	1	1	0	1	propagate
1	0	0	1	0	propagate
1	0	1	0	1	propagate
1	1	0	0	1	generate
1	1	1	1	1	generate

$$S = A \oplus B \oplus C_i$$
$$= A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i + ABC_i$$
$$C_o = AB + BC_i + AC_i$$

2. Write the expressions for the intermediate signals: generate, delete and propagate for a binary adder and express sum and carry out in terms of the above.

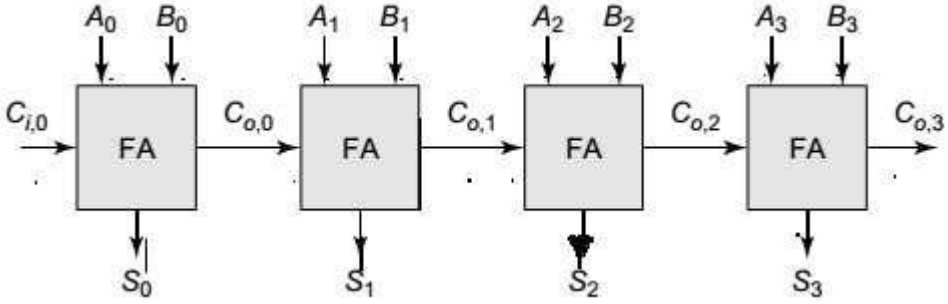
Generate (G) = AB

Propagate (P) = A ⊕ B

Delete = $\bar{A}\,\bar{B}$

$$C_o(G,P) = G + PC_i$$
$$S(G,P) = P \oplus C_i$$

3. Draw the topology of a four bit ripple carry adder.



4. What is the worst case propagation delay in an N bit ripple carry adder?

$$t_{adder} = (N\text{-}1)t_{carry} + t_{sum}$$

5. Write the dependency relationship between carry signals in a carry lookahead adder.

Carry boolean equations

$$C_i = G_i + P_i C_{i-1} = \overline{K_i + P_i \overline{C}_{i-1}}$$
$$\overline{C}_i = K_i + P_i \overline{C}_{i-1} = \overline{G_i + P_i C_{i-1}}$$

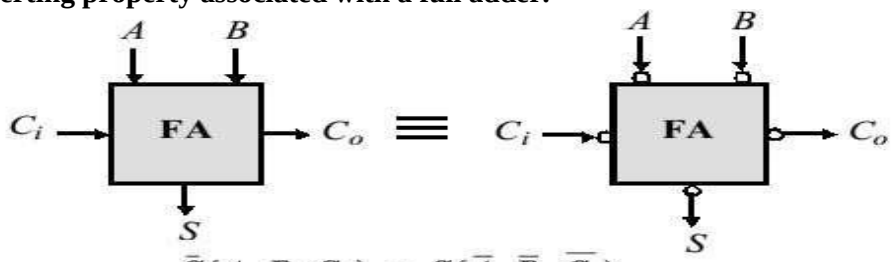
6. What are the main stages of an array multiplier?

The main stages of an array multiplier are: partial product generation, partial product accumulation and final addition.

7. What is meant by clustered voltage-scaling?

Clustered voltage-scaling is a method of distributing a wide range of supply voltages inside a block. In this technique, each path starts with the high supply voltage and switches to the low supply when delay slack is available.

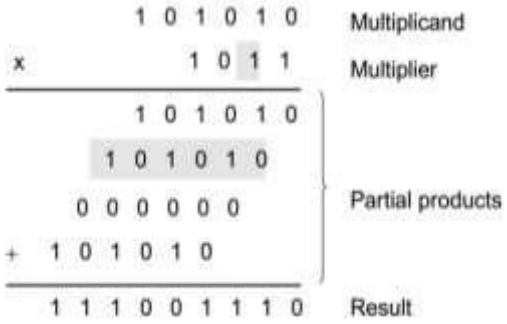
8. Write the inverting property associated with a full adder.



$$\overline{S}(A,B,C_i) = S(\overline{A},\overline{B},\overline{C_i})$$

$$\overline{C_o}(A,B,C_i) = C_o(\overline{A},\overline{B},\overline{C_i})$$

9. Illustrate binary multiplication using a simple example. Specify the bit size of the inputs and the partial products.



10. What is booth's recoding? Draw a partial product selection table for the same.

Booth's recoding reduces the number of partial products to at most half. It ensures that for every two consecutive bits at most one bit will be 1 or -1. Reducing the number of partial products is equivalent to reducing the number of additions, which leads to a speedup as well as an area reduction.

Partial Product Selection Table

Multiplier Bits	Recoded Bits
000	0
001	+Multiplicand
010	+Mutiplicand
011	+2xMultiplicand
100	-2xMultiplicand
101	-Multiplicand
110	-Multiplicand
111	0

11. What is the necessity of a level converter? Draw a simple circuit of the same.

When combining multiple supply voltages on a die, level converters are required whenever module at the lower power supply has to drive a gate at the higher voltage. If a gate supplied by V_{DDL} drives agate at V_{DDH}, the PMOS transistor never turns off, resulting in static current and reduced output swing. A level conversion performed at the boundaries of supply voltage domains prevents these problems.

12. What method is adopted to reduce power in idle mode?

A common method to reduce power in idle mode is clock gating. In this method, the main clock connection to a module is turned off (or gated) whenever the block is idle. However clock gating does not reduce leakage current in idle mode.

13. List the different considerations for designing a Ripple carry adder.

i. Propogation delay of ripple carry adder is linearly proportional to N.
ii. It is important to optimize t_{carry} than t_{sum}.
iii. Inverting all i/ps to a full adder results in inverted values for all o/ps.

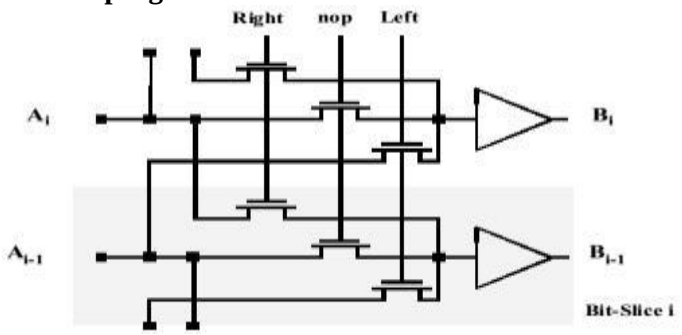
14. What are the draw backs of a static adder circuit.

i. Consumes large area.
ii. Circuit is slow.

15. What is the advantage of Dynamic Supply Voltage Scaling (DVS)?

Lowering the clock frequency when executing the reduced workloads reduces the power but does not save energy- every operation is still executed at the high voltage level. However if both supply voltage and frequency are reduced simultaneously, the energy is reduced. In order to maintain the required throughput for high workloads and minimize energy for low workloads, both supply and frequency must be dynamically varied according to the requirements application that is currently being executed. This technique is called Dynamic Supply Voltage Scaling (DVS).

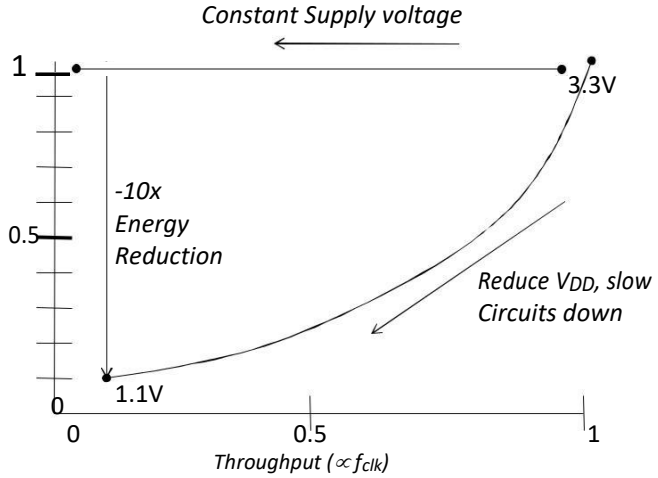
16. Draw the circuit of one bit programmable shifter



17. Tabulate various power minimization techniques in datapath structures.

	Design Time	**Sleep Mode**	**Run Time**
Active Transistors	Lower V_{DD}, Multi V_{DD} Tansistor Sizing Logic Optimization	Clock Gating	Dynamic Voltage Scaling
Leakage Transistors	Multi V_{th}	Sleep transistors	Variable V_{th}

18. Draw the energy/operation versus throughput curve for constant and variable supply voltage operation.



19. What are the parts of a DVS system? Also draw a figure for the same. A practical implementation of the DVS system consists of the following:

- A processor that operate at a wide variety of supply voltages.
- A power regulation loop that sets the minimum voltage necessary for operation at a desired frequency
- An operating system that calculates the desired frequencies to meet required throughputs and task Completion deadlines.

20. Illustrate threshold voltage control in an inverter.

Substrate bias is the control knob that allows us to vary the threshold voltages dynamically. In order to do so, we have to operate the transistors as four- terminal devices. Variable threshold voltage scheme can accomplish a variety of goals:

- It can lower the leakage in standby mode
- It can compensate for threshold voltage variations across the chip during normal operation of the circuit
- It can throttle the throughput of the circuit to lower both the active and leakage power based on performance requirements

21. What is the total time delay for a ripple carry Adder.

$T_{adder} = (N-1)\ t_{carry} + t_{sum}$.

22. Write down the Expression for the total propogation delay in an n bit carry bypass Adder.

$T_p = t_{set\ up} + M\ t_{carry} + (N/M-1)\ t_{bypass} + M\ t_{carry} + t_{sum}$.

23. Why is static adder circuit slow ?

A static adder ckt is slow as,

(i) Long chains of series PMOS transistors are present in both carry & Sum generation circuit.

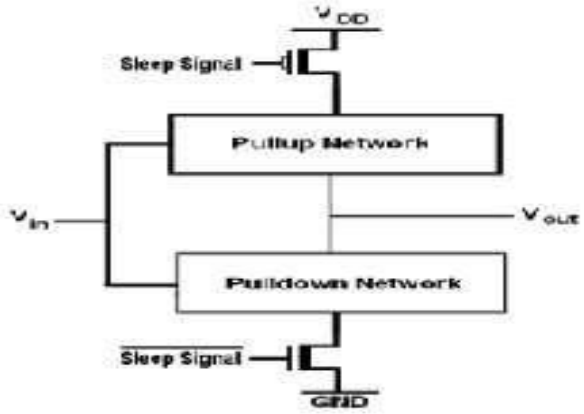
(ii) Intrinsic load capacitance of the C_o signal is large & consists of 2 diffusion & 6 gate

capacitances plus the wiring g capacitances.

(iii) Carry generation ckt requires 2 inverting stages per bit.

(iv) Sum generation ckt requires an extra logic stage

24. Draw the structure of a sleep transistor.



25. What is the advantage of Dynamic adder design?

Reduced capacitance of dynamic circuitry results in substantial speed up over static implementation.

26. **Determine propagation delay of n-bit carry select adder. (May/June 2016)**

$t_{add} = t_{setup} + M\ t_{carry} + (N / M)\ t_{max} + t_{sum}$

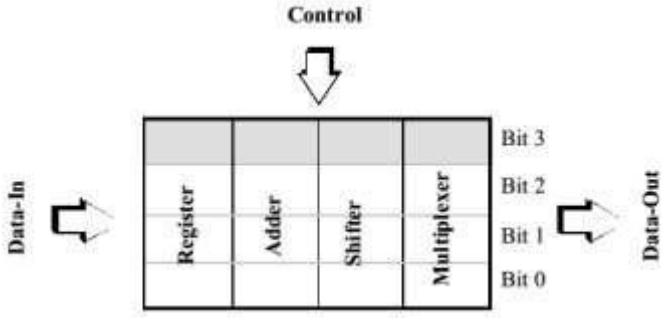
where t_{setup},t_{sum},t_{max} are fixed delays. N and M represents the total number of bits and no.of bits per stage respectively. t_{carry} is the delay of carry through a single full adder cell.

27. Give the application of high speed adder. (April / May 2017)

High speed Adders will reduce the hardware complexity and make justice with Speed Power,Area and Accuracy metrics. Adders are one of the key components in arithmetic circuits. Approximation can increase performance or reduce power consumption with a simplified or inaccurate circuit in application contexts where strict requirements are relaxed. The potential application is in the DSP application for portable devices such as cell phones and laptops.

28. Draw a bit sliced datapath organization / What is meant by bit-sliced data path organization? List out the components of data path. (April / May 2017)

Datapaths are often arranged in bit sliced organization instead of operating on single-bit digital signals. The data in a processor are arranged in a word based fashion. A 32 bit processor operates as data words that are 32bits word wide. This is reflected in the organization of datapath. Since the same operation frequently has to be performed on each bit of the data word, the datapaths consist of 32 bit slices, each operating on single bit, hence the term bit-sliced.



29. Write the principle of any one fast multiplier? (Nov/Dec 2016)

Booth multiplier is a radix -4 multiplication scheme , which examines 3 bits of the multiplicand at a time to determine whether to add 0,1,-1,2,-2 of that rank of the multiplicand.

PART B- C312.4

1. Explain worst case propagation delay of ripple carry adder with a suitable example.

2. What is the simplest approach to design a full adder circuit? What are its drawbacks?

3. Describe the implementation of a transmission gate based adder.

4. Describe the implementation of a Manchester Carry chain adder.

5. Describe the implementation of a carry bypass adder or carry skip adder.

6. Describe the implementation of a carry select adder.

7. (a)Explain the concept of a carry look ahead adder with neat diagram.(**May/June 2014) (Nov/Dec 2016)**

(b) discuss the details about speed and area trade off **(April/May 2017)**

8. Explain the concept of a high speed adder. **(Nov/Dec 2016)**
7. Illustrate the partial product generation logic associated with a multiplier.
8. Illustrate the various schemes for implementing partial product accumulation.
9. What are the methods adopted to perform division in a digital IC? Make a comparison between them.
10. Explain the structure of a Barrel Shifter. (**April/May 2015, Nov/Dec 2015)**
11. What is the design approach in a logarithmic shifter?
12. Illustrate various Design-Time power reduction techniques.
13. Illustrate various Run-time power management schemes.
14. How can power be reduced in the standby mode?
15. Design a 16 bit carry bypass and carry select adder and discuss their features. **(May/June 2016)**
16. Design a 4 X 4 array multiplier and write down the equation for delay. **(May/June 2016)**

17.Explain the operation of booth multiplication with suitable examples? Justify how booth algorithms speed up the multiplication process. **(Nov/Dec 2016)**

18.Explain the concept of modified booth multiplier with suitable example**(April/May 2017)**

UNIT V IMPLEMENTATION STRATEGIES
PART A- C312.5

1. What is an FPGA? (Nov/Dec 2014)

FPGA is Field Programmable Gate Array that consists of an array of anywhere from 64 to 1000s of logic gate groups that are sometimes called configurable logic blocks.

2. What is SOG?

A channelless gate-array is called sea-of-gates (SOG) array. The core area of the die is completely filled with an array of base cells (the base array).

3. Compare FPGA and CPLD?

CPLD's have a much higher capacity than simple PLDs, permitting more complex logic circuits to be programmed into them. A typical CPLD is equivalent of from 2 to 64 simple PLDs. The development of these devices followed simple PLD as advances in technology permitted higher density chips to be implemented. There are several forms of CPLD, which vary in complexity and programming capability. CPLDs typically come in 44 to 160 pin packages depending on the complexity.

FPGA are different from simple PLDs and CPLDs in their internal organization and have the greatest logic capacity. FPGAs are consists of an array of anywhere from 64 to 1000s of logic gate groups that are sometimes called logic blocks. Two basic classes of FPGAs are fine grained and course grained .The course grained FPGA has large logic blocks and fine grained FPGAs has much smaller logic blocks. FPGAs are come in packages up to 1000 pins or more.

4. Differentiate CBIC & Gate array logic?

CBIC	Gate array logic
Cell-based IC uses predesigned logic cells (AND gates, OR gates, multiplexers, and flip-flops, for example)	In a gate array (GA) or gate-array–based ASIC the transistors are predefined on the silicon wafer.
CBIC means a standard-cell–based ASIC	it is often called a masked gate array (MGA).
The standard-cell areas in a CBIC are built of rows of standard cells. The standard-cell areas may be used in combination with larger predesigned cells, known as megacells.	The logic cells in a gate-array library are often called macros.

5. List out three main parts of FPGA & what is PMS?

- CLB-Configurable Logic Block
- IOB-Input Output Block
- PMS-Programmable Switch Matrix

6. List the types of ASIC?/ State the different types of ASICs. (May/June 2014)

- Full-Custom ASICs
- Semicustom ASICs :

– Standard-Cell–Based ASICs

– Gate-Array–Based ASICs

- Channeled Gate Array
- Channelless Gate Array
- Structured Gate Array

- Programmable ASICs , for which all of the logic cells are predesigned and none of the mask layers are customized.

– Programmable Logic Devices
– Field-Programmable Gate Arrays

7. What is Full custom ASIC?/What are the features of full custom ASIC? (April/May 2015)(May/June 2016)

To modify according to a customer's individual requirements, All mask layers are customized in a full-custom ASIC

i. Generally, the designer lays out all cells by hand
ii. Some automatic placement and routing may be done
iii. Critical (timing) paths are usually laid out completely by hand

Full-custom design offers the highest performance and lowest part cost (smallest die size) for a given design.The manufacturing lead time (the time it takes just to make an IC—not including design time) is typically eight weeks for a full-custom IC.

8. Write the objectives and Goals of System Partitioning?

The goal of partitioning is to divide this part of the system so that each partition is a single ASIC. To do this we may need to take into account any or all of the following objectives:

- A maximum size for each ASIC
- A maximum number of ASICs
- A maximum number of connections for each ASIC
- A maximum number of total connections between all ASICs

9. What is JTAG?

Joint Test Action Group (*JTAG)*

10. What is fully PCI in Spartan-II FPGA?

Fully Peripheral Component Interface (PCI) used to interface components

11. Differentiate fine-grain and coarse-grain architecture of FPGA

Fine-grained Architecture	Coarse-grained Architecture
Manipulate data at the bit level	Manipulate groups of bits via complex functional units such as ALUs (arithmetic logic units) and multipliers
Designers can implement bit manipulation tasks without wasting reconfigurable resources	Reconfigurable resources are wasted during data manipulation
For large and complex calculations numerous fine-grained PEs are required to implement a basic computation	Fewer coarse-grained PEs are required to implement a basic computation
Much slower clock rates	Faster
Extremely costly relative to coarse-grained architectures	Less Expensive
Supports partial array configuration and is dynamically reconfigurable during application execution.	Both partially and dynamically reconfigurable

12. State the Xilinx FPGA design flow.

- Specification
- VHDL description - Functional simulation
- Synthesis - Post-synthesis simulation
- Implementation - Timing simulation
- Configuration - On chip testing

13. What are the different types of interconnections present in Xilinx FPGA?

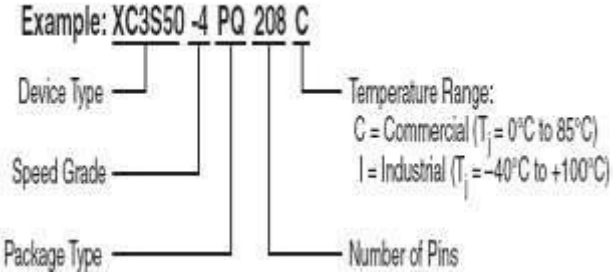
Direct interconnect: Adjacent CLBs are wired together in the horizontal or vertical direction. The most efficient interconnect.

General-purpose interconnect: used mainly for longer connections or for signals with a moderate fan-out.

Long line interconnect: for time critical signals (e.g. clock signal need be distributed to many CLBs)

14. What is meant by speed grading?

Most of the FPGA header short chip according to speed is called speed binning or speed grading. According to Xilinx FPGA product, The speed grade specify the transistor switching speed that determines how quickly internal clocked circuits can be activated.



15. What is meant by BIDA?

The Bidirectional Interconnect Buffers(BIDA) restore the logic level and logic strength on long interconnect paths.

16. Define OEM?

For any ASIC, a designer needs design-entry software, a cell library and physical design software. Often designers buy that software from FPGA vendor. This is called an Orginal Equipment Manufacturer (OEM) arrangement.

17. What are the advantages and disadvantages of FPGA compared to ASIC?

FPGA	ASIC
Faster time-to-market since none of the mask layers are customized	Full custom capability for design since device is manufactured to design specs
Simpler design cycle due to software that handles much of the routing, placement, and timing	Design cycle is not simple.
Field reprogramability - A new bit stream can be uploaded remotely	Field reprogramability is not possible
Design turnaround is a few hours	Two days to two weeks

18. Define segmented Channel routing?

FPGA is a channeled architecture. The logic modules which implement various types of logic functions are placed in predefined rows. Channels are defined in between rows of logic modules for routing of nets. The rows of logic modules are called tracks. The tracks are divided into different segments which can be connected together by programming a horizontal antifuse. Each input and output of a logic module is connected to a dedicated vertical segment. Cross antifuses are located at the crossing of each horizontal and vertical segment. Programming these antifuses produces a bi-directional connection between the horizontal and vertical segments for routing of nets via channels. This structure of FPGA is called segmented channel routing.

19. Differentiate between Altera MAX 9000 and Altera FLEX interconnects architecture?

The MAX 9000 is a coarse-grained architecture. Complex PLDs with arrays that are themselves arrays of macrocells have a dual-grain architecture. The FLEX architecture is of finer grain than the MAX arrays because of the difference in programming technology. The FLEX horizontal interconnect is much denser than the vertical interconnect creating an aspect ratio of 10:1.

20. List the advantages of Global routing. (May/June 2014)

We typically global route the whole chip (or large pieces if it is a large chip) before detail routing the whole chip (or the pieces). There are two types of areas to global route: inside the flexible blocks and between blocks.

The goal of global routing is to provide complete instructions to the detailed router on where to route every net. The objectives of global routing are one or more of the following:

- Minimize the total interconnect length.
- Maximize the probability that the detailed router can complete the routing.
- Minimize the critical path delay.

21. What are feedthrough cells? State their uses. (May/June 2016)

The term feedthrough cells can refer either to a piece of metal that is used to pass a signal through a cell or to a space in a cell, waiting to be used as a feed through.

22.What is the standard cell-based ASIC design?(Nov/Dec 2016)

In cell based design, the designer reuses the cells that have already been designed and stored in the library as a part of the current design. Cell – based IC used predesigned logic cells(AND gates, OR gates, multiplexers and flipflop). CBIC means standard cell based ASIC. The standard-cell areas in a CBIC are built of rows of standard cells. The standard-cell areas may be used in combination with larger predesigned cells known as megacells.

23. What is an antifuse? State its merits and demerits. (Nov/Dec 2016)

An antifuse is an electrical device that performs the opposite function to a fuse. Whereas a fuse starts with a low resistance and is designed to permanently break an electrically conductive path (typically when the

current through the path exceeds a specified limit), an antifuse starts with a high resistance and is designed to permanently create an electrically conductive path (typically when the voltage across the antifuse exceeds a certain level).

Disadvantage: The size of an antifuse is limited by the resolution of the lithography equipment used to makes ICs. The Actel antifuse connects diffusion and polysilicon, and both these materials are too resistive for use as signal interconnects.To connect the antifuse to the metal layers requires contacts that take up more space than the antifuse itself, reducing the advantage of the small antifuse size. However, the antifuse is so small that it is normally the contact and metal spacing design rules that limit how closely the antifuses may be packed rather than the size of the antifuse itself.

Advantages: There are two advantages of a metal–metal antifuse over a poly–diffusion antifuse.

The first is that connections to a metal–metal antifuse are direct to metal—the wiring layers.

Connections from a poly–diffusion antifuse to the wiring layers require extra space and create additional parasitic capacitance.The second advantage is that the direct connection to the low-resistance metal layers makes it easier to use larger programming currents to reduce the antifuse resistance.Average QuickLogic metal– metal antifuse resistance is approximately 80 W (with a standard deviation of about 10 W) using a programming current of 15 mA as opposed to an average antifuse resistance of 500 W (with a programming current of 5 mA) for a poly–diffusion antifuse.

24. What is meant by CBIC? **(April/May 2017)**

Cell – based IC used predesigned logic cells(AND gates, OR gates, multiplexers and flipflop). CBIC means standard cell based ASIC. The standard-cell areas in a CBIC are built of rows of standard cells. The standard-cell areas may be used in combination with larger predesigned cells known as megacells.

25. Name the elements in a Configurable Logic Block**(April/May 2017)**.

Flip flops to store data and Look up tables and Multiplexers to implement logic.

PART B- C312.5

1. With design flow, explain the sequence of steps involved in the ASIC design process.
2. Explain about the different types of ASIC with neat diagram **(April/May 2017)**
3. Describe the architecture of FPGA with Configurable Logic Block and Programmable interconnect technology. **(April/May 2015) (Nov/ Dec 2016)**
4. (a) Explain the Configurable Logic Block and IO block of Xilinx XC4000 FPGA.
   (b) List the features of Xilinx XC4000 FPGA.
5. (i) Describe Gate-Array based ASIC's with neat diagrams. (8)
   (ii) With a neat Flowchart, explain the ASIC design flow. (8) **(May/June 2014)**
6. (i) Explain features of semi-custom ASIC and its types.(8) **(April/May 2015)**
   (ii)Write explanatory notes on FPGA (8) **(May/June 2014)**
7. Explain FPGA interconnect routing procedures.
8. Write brief notes on **(May/June 2016) (Nov/ Dec 2016)**
   a. Semi-custom ASIC
   b. Full Custom ASIC
9. With neat sketch explain the CLB,IOB and programmable interconnects of an FPGA device **(May/June 2016)**
10. Write short notes on Standard cell design and cell libraries.
11. (a)Explain about building block architecture of FPGA
    (b)Write short notes on routing procedures involved in FPGA interconnects**(April/May 2017)**