UNIT-I: THE 8086 MICROPROCESSOR

PART-A

1.What are the types of instruction sets of 8086 microprocessor?

There are eight types of instructions.

Data copy/Transfer instructions, Arithmetic & Logical instructions, Branch instructions Loop instructions, Machine control instructions, Flag manipulation instructions Shift & rotate instructions, String instructions

2.What are flag manipulation instructions?

The instructions that directly modify the flags of 8086 are called as the flag manipulation instructions.E.g.: CLC -clear carry flag, CMC - complement carry flag, STC- set carry flag and CLD- clear direction flag

3.Write a program to generate a delay of 100 ms using 8086.

The required delay Td=100 ms

Instructions selected	states for execution
MOV CX, COUNT	4
L1 :DEC CX	2
NOP	3
JNZ L1	16

No. of clock cycles for execution of the loop once =2+3+16 = 21

Time required to execute the loop once is 21*.1=2.1 micro sec.

COUNT=required delay (td),N* T

Required count = 100*10^-3

2.1*10^-6

= 47.619*10^3 = 47619 = BA03

4.Which interrupt has got the highest priority among all the external interrupts?

The Non-Maskable Interrupt pin of 8086 has got the highest priority among the external interrupts.

5.Define a MACRO.

A number of instructions appearing again & again in the main program can be assigned as a macro definition (i.e.) a label is assigned to the repeatedly appearing string of instructions.

The process of assigning a label or macro name to the string is called defining a macro. A macro within a macro is called a nested macro.

6.What is the segment registers present in 8086? (Nov/Dec 2016)

There are four segment registers in 8086.They are Code Segment register (CS), Data Segment register (DS), Extra Segment register (ES),Stack Segment register (SS).

7.What do you mean by instruction pipelining?

While the execution unit executes the previously decoded instruction, the Bus Interface Unit fetches the next instruction and places it in the prefetched instruction byte queue. This forms a pipeline.

8.What are the advantages of the segmented memory scheme in 8086?

The following are the advantages of the segmented memory scheme

1) Allows the memory capacity to be 1 Mbytes although the actual addresses to be handled are of 16-bit size.

2) Allows the placing of code, data and stack portions of the same program in different parts of memory, for data and code protection.

3) Permits a program and/or its data to be put into different areas of memory each time program is executed.

9.What is the use of the Trap flag in the flag register of 8086?

When the Trap flag is set, the processor enters the single step execution mode. A trap interrupt is generated after execution of each instruction. The processor executes the current instruction and the control is transferred to the Trap interrupt service routine.

10.List the instruction formats in 8086 instruction set.

There are six general formats of instruction in 8086.They are

One byte instruction, Register to Register, Register to/from Memory with no Displacement, Register to/from memory with Displacement, Immediate operand to Register, Immediate operand to Memory with 16-bit Displacement.

11.What are the addressing modes of sequence control transfer instructions in 8086? Give example.

The addressing modes are Immediate eg: Mov AX, 0005H, Direct eg: Mov AX, [5000H], Register eg:Mov BX,AX,Register Indirect eg:Mov AX,[Bx],Indexed eg: Mov AX,[SI],Register

Relative eg:Mov AX,50H[BX],Based Indexed eg: Mov AX, [Bx] [SI], Relative Based Indexed eg: Mov AX, 50H [BX] [SI].

12.How is the physical address generated in 8086? (or) How 16 bit address is converted into 20 bit address in 8086? (Nov/Dec 2013)

The content of the segment register called as segment address is shifted Left bit-wise four times and to this result, content of an offset register also called as offset address is added, to produce a 20-bit physical address.

eg: segment address →1005H
Offset address →5555H
Segment address →0001 0000 0000 0101
Shifted by 4 bit positions →0001 0000 0000 0101 0000
+
Offset address →0101 0101 0101 0101
Physical address →0001 0101 0101 1010 0101
1 5 5 A 5

13.What are the differences between 8085 and 8086? (Nov/Dec 2013)

S.No	8085	8086
1	8-bit microprocessor	16-bit microprocessor
2	It is capable of addressing 2^{16} memory locations	It is capable of addressing 2^{20} memory locations
3	Low speed	High speed
4	It can be configured only in single processor mode	It can be configured in single processor mode(Minimum) and Multiprocessor mode(Maximum)

14.Explain XLAT instruction.

- The XLAT (Translate) instruction replaces a byte in the AL register with a byte from a 256-byte, user coded translation table.
- XLAT is useful for translating characters from one code to another like ASCII to EBCDIC and ASCII to HEX etc.

15.Draw the PSW format for 8086 / List the flags in 8086 and state its functions. (May/June 2014, 2016, Nov/Dec 2016).

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AF	U	PF	U	CF

U : Undefined
CF : Carry flag - Set by carry out of MSB
PF : Parity flag - set if result has even parity
AF : Auxiliary carry flag - used for BCD operation
ZF : Zero flag - set if result = 0
SF : Sign flag - set if result is –ve.
TF : Trap flag - set to enable single step execution mode.
IF : Interrupt flag - set to enable interrupt
DF : Direction flag - set to enable auto decrement mode for string operation
OF : Overflow flag - used for signed arithmetic operation

16.What is the function of parity flag? (Nov/Dec 2013)

The parity flag is set, if the result of the byte operation or lower byte of the word operation contains an even number of ones.

17.Give the operation of CBW and TEST instructions of 8086? (Nov/Dec 2013)

CBW instruction converts the byte in AL to word value in AX by extending the sign of AL throughout the register AH.TEST instruction performs logical AND operation of the two operands updating the flag registers without saving the result.

18.What do you mean by addressing modes? (May/Jun 2014)

The addressing modes clearly specify the location of the operand and also how its location may be determined.

19.What is meant by a vectored interrupt? (May/Jun 2014)

There is an interrupt vector table which stores the information regarding the location of interrupt service routine (ISR) of various interrupt. Whenever an interrupt occurs the memory location of ISR is determined using the vector table and the program control branches to ISR after saving the flags and the program location (Instruction Pointer and Code Segment Register) in the stack.

20.Identify the addressing modes in the following instructions. (May/June 2014)

AND AL, BL **:** REGISTER ADDRESSING MODE
SUB AL, 24H **:** IMMEDIATE ADDRESSING MODE
MOV AL, (BP) **:** INDIRECT ADDRESSING MODE
MOV CX, 1245H **:** IMMEDIATE ADDRESSING MODE

21.What is an assembler? (Nov/Dec 2014)

The assembler translates the assembly language program text which is given as input to the assembler to their binary equivalents known as object code. The time required to translate the assembly code to object code is called access time. The assembler checks for syntax errors & displays them before giving the object code.

22.Calculate the physical address, when segment address is 1085 H and effective address is4537 H. (Nov/Dec 2015)

Physical address= 10* 1085 H + 4537 H = 14D87 H

23.Show how the 2 byte INT instruction can be applied for debugging. (Nov/Dec 2015)

INT 1 is called as single-step interrupt. When microprocessor executes INT 1 instruction, it will execute one instruction and stop. Then, it goes and examines the contents of registers and memory locations. If the contents are correct, the microprocessor executes the next instruction. INT 3 is called as break point interrupt. This is used to insert break points for debugging the program. The microprocessor executes the program up to the break point and then branches to break point Interrupt service routine(ISR).

25.Define Stack? (May/June 2016)

A stack pointer is a small register that stores the address of the last program request in a stack. A stack is a specialized buffer which stores data from the top down. As new requests come in, they "push down" the older ones.

PART-B

1.Explain the memory concepts of Intel 8086 and explain how data transfer takes place.
2.Explain the internal architecture of 8086 and explain the functions of each block in detail.**(Nov/Dec 2013,2016)**
3. Write an 8086 ALP to logically shift a 16 bit number stored in location starting at 8000H twice to the right. Store the result in A000 H.
4.Explain the different instruction used for input and output operation in I/O mapped I/O mode of 8086.
5.What are the data related addressing modes used in 8086? Explain each with neat diagrams.(10)
6.Explain the register organization of the 8086. Discuss how the physical address generation is carried out.
7.What is meant by memory segmentation? What are the advantages of memory segmentation?
8.Draw and discuss the interrupt structure of 8086. **(May/Jun 2014)**
9.Write an 8086 ALP to sort out any given ten numbers in ascending and descending order. **(Nov/Dec 2013)**
10. With a neat diagram explain the bus interfacing unit and execution unit available in 8086 microprocessor. **(Nov/Dec 2014) / (May/Jun 2014)**.
11. (i) Briefly explain the arithmetic group of instructions available in 8086 microprocessor. (8)
(ii) Briefly explain the assembler directives of 8086. (8) **(Nov/Dec 2014,2016).**
12. (i) Explain the architecture of Intel 8086 with the help of a block diagram. **(8) (Nov/Dec 2015).**
(ii)Briefly describe about addressing modes of 8086. (8) **(Nov/Dec 2014,2015,2016)**
13. Explain in detail about the interrupts and interrupt service routine of 8086.(16) **(Nov/Dec 2015)**
14. Define interrupts and their types. Write in detail about interrupt service routine. **(May/Jun 2016)**
15. Explain the Data transfer, arithmetic and branch instructions with examples. **(May/Jun 2016)**
16. Write an 8086 ALP to find the sum of numbers in an array of 10 elements. . **(May/Jun 2016)**

UNIT-II: 8086 SYSTEM BUS STRUCTURE

PART – A

1. What is meant by multiprocessor system?

If a microprocessor system contains two or more components that can execute instructions independently then the system is called as multi-processor system.

2. What are the architectures of multiprocessor system?

Loosely coupled architecture
Closely coupled architecture

3. What is closely coupled configuration?

If the processor supporting processor, clock generator, bus control logic, memory and I/O System, communicate shared memory then it is called closely coupled system.

4. What are the advantages of loosely coupled configuration?

1. Better system throughput by having more than one processor
2. A greater degree of parallel processing can be achieved
3. System structure is more flexible
4. A failure in one module does not cause any breakdown of the system.

5. What is meant by cross bar switch?

If the number of buses in a common bus system is increased, a point is reached at which there is a separate path available for each memory module. This interconnection is called as crossbar switch

6. What is bus? (Nov/Dec 2016)

A *bus* in a microprocessor-based system is defined as a group of separate wires which work together to perform a particular task. A microprocessor-based system, or microcomputer, has three buses which combine to transfer information between the microprocessor and other parts of the system, such as memory or input/output devices.

Address bus: a group of wires which selects the address of the source/destination for the data transfer. The address bus is an output from the microprocessor.

Data bus: a bi-directional group of wires used to transfer between the source and destination, one of which will normally be the microprocessor.

Control bus: a miscellaneous group of wires which is responsible for controlling and synchronizing the data transfer process.

7. Differentiate internal Vs external bus? (April/May 2016)

An internal bus or local bus and an external bus, also called the expansion bus. An internal bus enables communication between internal components such as a video cardand memory. An external bus is capable of communicating with external components such as a USB or SCSI device.

8. Compare closely coupled and loosely coupled configurations. (April/May 2016)

Closely coupled: If the processor supporting processor, clock generator, bus control logic, memory and I/O System communicate shared memory then it is called closely coupled system.

Loosely coupled: In a loosely coupled multiprocessor system each CPU has its own bus control logic and bus arbitration is resolved by extending this logic and adding external logic that is common to all the modules.

9. Name some techniques for reducing contentions

1. Local memories
2. Better interconnection network
3. Cache memory
4. Memory Allocation

10. What is meant by bus arbitration?

The mechanism which decides the selection of current master to access bus is known as bus arbitration.

11. What are the advantages of Daisy Chaining?

1. It is simple and cheaper method
2. It requires the least number of lines and this number is independent of the number of masters in the system

12. What is meant by Numeric Processor?

The numeric processor 8087 is a coprocessor which has been specially designed to work under the control of the processor 8086 and to support additional numeric processing capabilities

13. What is meant by instruction Queue?

It is of 6 bytes length which is used to speed up execution of programs by pre-fetching six bytes of instruction in advance from the memory.

14. On which data types can memory operands operate?

1. Word integer 2. Short integer 3. Long integer 4. Packed BCD 5. Short real 6. Long Real,
7. Temporary real

15. List some of the instructions format

1. Data Transfer Instructions 2. Arithmetic Instructions 3. Compare Instructions 4. Transcendental Instructions 5. Load Constant Instructions 6. Processor control Instructions

16. What is a co-processor? (Nov/Dec 2013)

The 8086/8088 must be supplemented with co-processors that extends the instruction set to allow the necessary special computations to be accomplished more efficiently. Eg: 8087 Numeric Data Processor.

17. What is a Floating point Coprocessor? (Nov/Dec 2013)

The floating point coprocessor uses real data types or floating point types of the following format:
Real data $X=\pm 2^{exp} \times$mantissa, which may vary from extremely small to extremely large values.

18. What are advantages of coprocessor? (May/Jun 2014)

The co-processors are supplementary processors which can fetch operands and execute it**.** It can read CPU status and queue status, make bus and interrupt request, receive reset and ready signals, receive bus grants, maintain an instruction queue and decode the external opcode.

19. What is meant by loosely coupled configuration? (May/Jun 2014)

In a loosely coupled multiprocessor system each CPU has its own bus control logic and bus arbitration is resolved by extending this logic and adding external logic that is common to all the modules.

20. Explain the function of TEST pin in 8086

This input is examined by a "WAIT" instruction. When the processor executes WAIT instruction it enters into wait state (Idle state). If the TEST pin goes low, the processor will come out from the idle state and continues the execution; otherwise it remains in an idle state.

21. How does the main processor distinguish its instructions from the co-processor instructions when it fetches the instructions from memory?

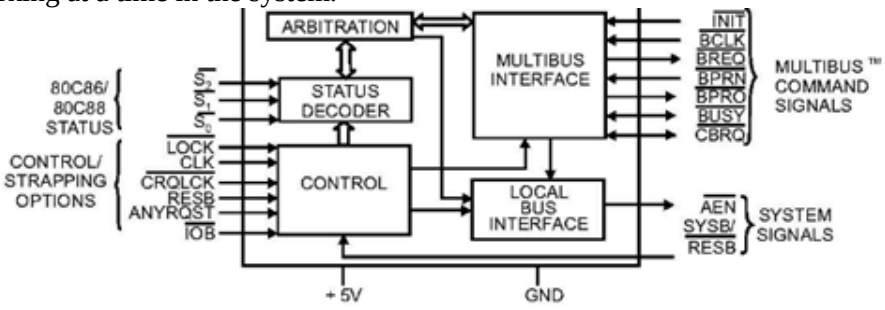
When main processor encounters the start of the mnemonic as ESC instruction, the instruction is for co-processor.

22. What is multi programming? (Nov/Dec 2015)

Multiprogramming is a rudimentary form of parallel processing in which several programs are run at the same time on a uniprocessor. Since there is only one processor, there can be no true simultaneous execution of different programs. Instead, the operating system executes part of one program, then part of another, and so on. To the user it appears that all programs are executing at the same time.

23.Schematically show, how synchronization is made between 8086 and its co-processor.(Nov/Dec 2015)

Coprocessors are unable to work independently as they are unable to fetch the code from memory and thus they work under the control of the main processor. Additional hardware elements like bus controllers and bus arbiters are used to coordinate the activities of the number of coprocessors working at a time in the system.



24.What is machine cycle? (Nov/Dec 2016)

It is the time required by the microprocessor to complete the operation of accessing the memory devices or I/O devices. In machine cycle various operations like opcode fetch, memory read, memory write, I/O read, I/O write are performed.

25.What is purpose of decoder in EU?

Decoder in EU transmits instruction fetched from memory into series of actions ,which EU caries out.

PART-B

1.Discuss the architectural features of 8086 that support multiprocessor design. (10)

2.Explain the closely coupled configuration of multi-processor configuration with suitable diagram. **(May/Jun 2014**Explain in detail about system bus timing of 8086/8088.**(Nov/Dec 2016)(April/May 2016)**

3.Explain the maximum mode and minimum mode of operation of 8086. **(Nov/Dec 2013)**

4.Differentiate closely coupled configuration and loosely coupled configuration. (6) **(Nov/Dec 2013)**

5.Draw the pin details of 8086 and explain the function of each pin.

6.Give the functions of NMI, BHE and TEST pins of 8086. (4) **(Nov/Dec 2013)**

7.With neat diagram explain the minimum mode of operation of 8086.(16) **(Nov/Dec 2015)**

8.Define loosely coupled system. Explain the schemes used for establishing priority.(16) **(Nov/Dec 2015)**

9. Explain the following:(i) Multiprocessor system (ii) Coprocessor (iii) Multiprogramming (iv) Semaphore **(April/May 2016)**

10. Discuss about the multiprocessor configuration of 8086?**(Nov/Dec 2016)**

UNIT-III I/O INTERFACING

PART –A

1. Why the 8255A is designed so that only the bits in PORT C can be set/reset?

Since the pins are designed to activate for selecting Port A and Port B.

2. What is the use of BSR mode in 8255

It is used for setting and Reset the Bits

3. How many I/O devices with a word length of 1 bit can be connected to 8255 PPI

EIGHT I/O devices can be connected to 8255 PPI

4. How does 8255 PPI discriminate between the memory section data and I/O section data

The 8255 PPI discriminate between memory section data and I/O Section by use of the Address lines and by use of the decoder.

5. What is the function of STB and OBF signal in the 8255 when programmed for mode –1 operation?

The input device activates this signal to indicate CPU that the data to be read is already sent on the port lines of 8255 port.

6. Name the major block of 8259 Programmable Interrupt Controller.

There are three major blocks1. Inrerrupt service reg 2. Priority resolver 3. Interrrupt Request Register 4. Interrupt Mask Reg

7. What are the modes of operation of 8259 interrupt Controller?

1. Fully Nested Mode 2. Special Fully Mode 3. Rotating Priority Mode 4. Special masked Mode
5. Polled Mode

8. What is the maximum number of devices that can be connected to interrupt mode?

Devices can be connected in the interrupt mode.

9. Mention the function of SP/EN signal in the 8259 PIC.

With the help of SP/EN signal it can either be operated in Master mode and Salve Mode

10. Why CAS2-CAS0 lines on 8259 PIC are bi-directional?

CAS2-CAs0 is used for selecting one of the possible slaves that can be connected.

11. What is Key bouncing.(May/June 2016).

if you press a key -just once- you will see on the Logic analyzer more than one pulse. to over come this you had to use a low pass filter , you can just out a capacitor to gound to filter the small pulses wich follows the main pulse.

12. What is the use of the READY input of the DMA controller?

When the READY PIN is high the data connected to the external devices can be activated.

13. What are the modes in DMA?

Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode, Cascade Mode

14. How DMA is initiated?(Nov/Dec 2016).

The 8086 microprocessor receives bus requests through its HOLD pin and issues grants from the hold acknowledge (HLDA) pin. A request is made when a potential master sends a 1 to the HOLD pin. Normally, after the current bus cycle is complete the 8086 will respond by putting a 1 on the HLDA pin. When the requesting device receives this grant signal it becomes the master. It will remain master until it drops the signal to the HOLD pin, at which time the 8086 will drop the grant on the HLDA pin.

15. List the four possible modes of operation in 8237 DMA controller.

1. Rotating Priority Mode 2. Fixed Priority Mode 3. Extended Write Mode 4. TC Stop Mode
5. Auto Load Mode

16. What is an USART.

Universal Synchronous and asynchronous Receiver and Transmitter is used for transmitting and Receiving data.

17. What is the drawback of memory mapped I/O?(Nov/Dec 2016)

The big disadvantage of memory-mapped I/O devices is that they consume addresses in the memory map. Generally, the minimum amount of space you can allocate to a peripheral (or block of related peripherals) is a four kilobyte. Therefore, a few independent peripherals can wind up consuming a fair amount of the physical address space.

18. List the advantages and disadvantages of parallel communication over serial communication (May/June2016).

parallel data transfer refers to the type of data transfer in which a group of bits are transferred simultaneously while serial data transfer refers to the type of data transfer in which a group of data bits are transferred one bit at a time. so that means that the amount of data transferred serially is less that the data transferred parallelly per second. serial data transfer requires less cables so if the data has to be transmitted over longer distances serial data transfer is preferred.

19. What are the operating modes of 8255? (Nov/Dec 2013)

Mode-0, Mode-1 and Mode-2.

20. What is bus stealing? (Nov/Dec 2013)

During DMA data transfer, the I/O component connected to the system bus is given control of the system bus for a bus cycle. This is called bus stealing or cycle stealing.

21. What are the advantages of Programmable Interval Timer/Counter IC? (May/Jun 2014)

- Interrupt a time sharing operating system at evenly spaced intervals.
- Output precisely timed signals with programmed period to an I/O device.
- Count the number of times an event occurs in an external experiment.
- Cause the processor to be interrupted after a programmable number of external events have occurred.

22. List the features of Memory Mapped I/O. (May/Jun 2014)

The device registers can be accessed and manipulated with any instruction or addressing mode. The maximum numbers of available memory locations are reduced.

23. What is key debouncing? What are the methods to detect the debouncing? (Dec 2014/June 2014)

Whenever a mechanical push-button is pressed or released once, the mechanical components of the key do not change the position smoothly, rather it generates a transient response. These transient variations may be interpreted as the multiple key pressure and responded accordingly by the microprocessor system. To avoid this problem, two schemes are suggested: the first one utilizes a bistable multivibrator at the output of the key to debounce . The other scheme suggests that the microprocessor should be made to wait for the transient period (usually 10ms), so that the transient response settles down and reaches a steady state.

24. List the operating modes of 8255 A and 8237 A. (Nov/Dec 2015)

Operating modes of 8255 A:

1.BSR mode: In this mode, any of the 8 bits of port C can be set or reset.

2.I/O mode: Mode 0 (Basic I/O mode), Mode 1 (Strobed I/O mode) and Mode 2 (Strobed bidirectional mode).

Operating modes of 8237 A:

1.Rotating Priority Mode 2. Fixed Priority Mode 3. Extended Write Mode

3.TC Stop Mode, 5. Auto Load Mode

25. What frequency transmit clock (TXC) is required by an 8251 in order for it to transmit data at 4800 baud with a baud rate factor of 16? (Nov/Dec 2015)

Baud rate factor = (TXC) / (Desired Baud Rate)

(TXC)= Baud rate factor X Desired Baud Rate = 16 X 4800= 76,800 Hz

PART – B

1.With a neat block diagram explain the function of each block of a programmable interrupt controller

2.Explain the procedure of Interfaceing A/D and D/A converter with a microprocessor**.(Nov/Dec 2016)(April/May 2014)**

3.(i) Explain the mode 0 operation of 8255 Programmable Peripheral interface. (8) **(May/Jun 2014)**

(ii) Explain the different modes of operation of timer. (8)

4. Explain the internal architecture of 8237 Direct Memory Access Controller. **(May/Jun 2014)(Nov/Dec 2016)(May/June 2016)**

5.Draw the block diagram and explain the operations of 8251 serial communication interface.(16) **(Nov/Dec 2015) (Nov/Dec 2013)**

6. (Nov/Dec 2013) (Nov/Dec 2014)

7.Explain design of Traffic Light Controller using 8086 microprocessor in detail.

8.Discuss the operation of LCD display and LED display, by interfacing with 8086 microprocessor.

9.Design a microcomputer based on 8086 with 16k EPROM and 16K RAM.

10. Compare memory mapped I/O with I/O mapped I/O. Explain byte data and word data are need from ODD addressed locations and EVEN addressed locations.

11. With a neat block diagram explain programmable interval timer IC 8253(8). **(Dec 2014)(April/May 2014)**

12. Draw the block diagram of programmable interrupt controller and explain its operations.(16) **(Nov/Dec 2015)**

13. Draw and explain the block diagram of alarm controller**.(May/June 2016)**

UNIT-IV: MICROCONTROLLER

PART –A

1.Discuss the salient features of 8051 family of controllers?

- Eight-bit CPU with registers A (the accumulator) and B.
- Sixteen-bit program counter (PC) and data pointer (DPTR).
- Eight-bit program status word (PSW).
- Eight-bit stack pointer (SP).
- Internal ROM or EPROM (4 KB).
- Internal RAM (128 bytes)
- Four register banks (each 8 registers)
- 16 bytes, which may be addressed at bit level
- Eighty bits of general purpose data memory
- Two 16-bit timer / counters: T0 & T1
- Full duplex serial data receivers / transmitter (SBUF)
- Control registers: TCON, TMOD, SCON, PCON, IP and IE.
- Two external and three internal interrupt sources
- Oscillator and clock circuits

2.What is the size of RAM in 8051?

The size of the RAM is **128 bytes**

1. Four register banks (each 8 registers)
2. 16 bytes, which may be addressed at bit level
3. Eighty bits of general purpose data memory

3.How many ports are available in 8051 micro controller?

There are mainly four ports available in this 8051 micro controller. They are

Port0: serve as inputs, outputs, or, when used together, as a bi-directional low order address and as data bus for external memory.

Port1: has got no dual functions.

Port2: may be used as an input / output port similar in operation to port 1. The alternate use of port2 is to supply a high-order address byte in conjunction with the Port0 low-order byte to address external memory.

Port3: is an input / output pin similar to the Port 1. In this case each and every pin has an additional function.

PIN	ALTERNATE USE	SFR
P3.0 – RXD	Serial data input	SBUF
P3.1 – TXD	Serial data output	SBUF
P3.2 - INT0	External interrupt 0	TCON.1
P3.3 - INT1	External interrupt 1	TCON.3
P3.4 – T0	External timer 0 input	TMOD
P3.5 – T1	External timer 1 input	TMOD
P3.6 – WR	External memory write pulse	_
P3.7 - RD	External memory read pulse	_

4.State the function of RS1 and RS0 bits in the flag register of Intel 8051.

RS0 and RS1 are the D3 and D4 bits present in the 8-bit register of the PSW (Program Status Word).

RS1	RS0	DESC.
0	0	BANK 0 is selected from Internal ROM
0	1	BANK 1 is selected from Internal ROM
1	0	BANK 2 is selected from Internal ROM
1	1	BANK 3 is selected from Internal ROM

5.What is meant by microcontroller?

A device which contains the microprocessor with integrated peripherals like memory, serial ports, parallel ports, timer/counter, interrupt controller, data acquisition interfaces like ADC, DAC on single chip is called microcontroller.

6.List the flags of 8051 and give their usage.

Status flags: These flags are modified according to the result of arithmetic and logical operations.

1. Carry flag, 2. Auxiliary carry flag 3. Overflow flag 4. Parity flag

General purpose user flags: These flags can be set or cleared by the programmer as desired Flag 0, GF0, GF1

7.What happens in power down mode of 8051 microcontroller?

The memory locations of power down RAM can be maintained through a separate small battery backup supply so that the content of these RAM can be preserved during power failure conditions.

8.Compare the 8051, 8031 and 8751 microcontrollers.

8051	8031	8751
On-chip program memory(ROM) available -4KB	No on-chip ROM	On-chip program memory(EPROM) available

9.What is the difference between microprocessor and microcontroller? (May/Jun 2014)

S.No	Microprocessor	Microcontroller
1.	It has only CPU	It has CPU, memory, timers, parallel and serial I/O port on single chip
2.	It has few bit manipulating instructions	It has large number of bit manipulating instructions
3.	It has more number of instructions for transferring data from external memory.	It has only few instructions for transferring data form external memory.
4.	No special function registers are available	Special functions registers are available

10.List any applications of Microcontroller.

1.Building control(Fire detection),Industrial control (Process control),Motor speed control(Stepper motor control),Stand alone devices(Color Xerox machine),Automobile applications (Power steering)

11.What is the function of DPTR register?

The data pointer (DPTR) is the 16-bit address register that can be used to fetch any 8 bit data from the data memory space. When it is not being used for this purpose, it can be used as two eight bit registers, DPH and DPL

12.What is the significance of EA line of 8051 microcontroller? (May/Jun 2014) (Nov/Dec 2016)

When there is no on-chip ROM in microcontroller and EA pin is connected to GND, it indicates that the code is stored in external ROM.

13.What is the difference between MOVX and MOV? (Nov/Dec 2013)

The MOV instruction is used to access code space of on-cip ROM and MOVX instruction is used to access data space or external memory.

14.What are the different ways of operand addressing in 8051? (May/Jun 2016)

Immediate addressing mode ,Direct addressing mode, Register addressing mode, Register indirect addressing mode ,Indexed addressing mode

15.Mention some of the 8051 special function register.

ACC: Accumulator, B: B-Register, PSW: Program Status Word, SP: Stack Pointer, DPTR: Data Pointer, IE: Interrupt Enable, SCON: Serial Control, PCON: Power Control.

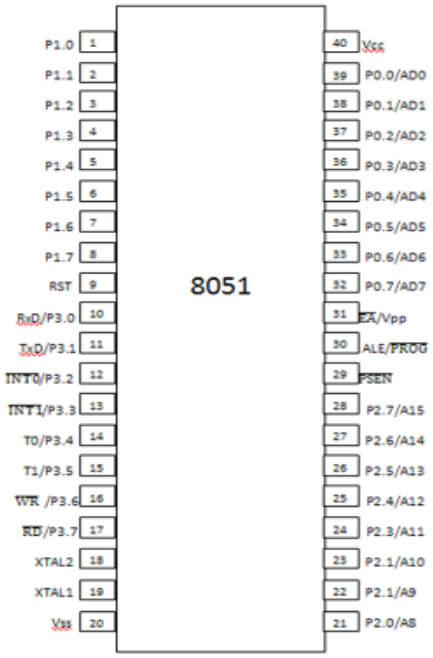
16.What is the function of XTAL 1 and XTAL 2 pins?

8051 has internal clock circuit. In this crystal of proper frequency can be connected to these two pins. XTAL 1 is connected to GND and oscillator signal is connected to XTAL 2.

17.Write an ALP to add the values ABH and 47H. Store the result in R1.

```
MOV A, #AB H
ADD A, #47 H
MOV R1, A
L1: SJMP L1
```

18.Draw the PIN diagram of 8051? (Nov/Dec 2016)



19.How is RAM memory space allocated in 8051?

- 32 bytes from 00 to 1F H is for register bank and stack.
- 16 bytes from 20H to 2FH is for bit addressable read/write memory
- 80 byte 30H to 7FH is for scratch pad

20.Differentiate overflow flag and carry flag.

Carry flag is used to detect error in unsigned arithmetic.

Carry flag is used to detect error in unsigned arithmetic.

21.List the SFRs involved in interrupt programming of 8051 (Nov/Dec 2014)

Interrupt priority (IP) Control registerIE Register (Interrupt Enable)

22.Why it is necessary to have external pull-up for port 0 in 8051? (Nov/Dec 2014)

When port 0 is used as an output port, the pin latches that are programmed to a 0 will turn on the lower FET, grounding the pin. All latches that are programmed to a 1 still float; thus, external pullup resistors will be needed to supply a logic high when using port 0 as an output port.

23.What is the difference between AJMP and LJMP instruction? (May/Jun 2014)

LJMP: LJMP (long jump) causes the program to branch to a destination address defined by the 16-bit operand in the jump instruction. Because a 16-bit address is used the instruction can cause a jump to any location within the 64KByte program space (216 = 64K). Some example instructions are:

LJMP LABEL_X ; Jump to the specified label

LJMP 0F200h ; Jump to address 0F200h

LJMP @A+DPTR ; Jump to address which is the sum of DPTR and Reg. A

AJMP: This is a special 8051 jump instruction, which allows a jump with a 2KByte address boundary (a 2K page)

24.How does the processor 8051 know whether on-chip ROM or external program memory is used? (May/Jun 2014)

EA (External Access) pin is grounded for accessing external program memory & PSEN (Program Store Enable) signal is activated to read a byte of instruction from External program memory. EA & PSEN signals are not used for accessing internal program memory. 8051 differentiates the external and internal program memory by using EA and PSEN signals.

25.Mention the number of register banks and their addresses in 8051. (Nov/Dec 2015)

There are four register banks, in each register bank there are eight 8 bit register available from R0 to R7. By default Bank 0 is selected. For Bank 0, R0 has address 00H and R1 has 07H. For selecting banks we use RS0 and RS1 bit of PSW.

RS1	RS2	Space in RAM
0	0	Bank0 00h-07h
0	1	Bank1 08h-0Fh
1	0	Bank2 10h-17h
1	1	Bank3 18h-1Fh

26.What is the jump range? (Nov/Dec 2015)

A JUMP or CALL instructions can replace the contents of the program counter with a new program address number that causes program execution to begin at the code located at the new address. The difference, in bytes, of this new address from the address in the program where the JUMP or CALL is located is called the range of the JUMP or CALL. There are three types of jump range.

Short jump range uses a single byte address. This address is a signed 8-bit number and allows the program to branch to a distance –128 bytes back from the current PC address or +127 bytes forward from the current PC address.

Absolute jump range allows a jump with a 2KByte address boundary (a 2K page)

Long jump range causes the program to branch to a destination address defined by the 16-bit operand in the jump instruction. Because a 16-bit address is used the instruction can cause a jump to any location within the 64KByte program space (2^{16} = 64K).

27. Write an 8051 ALP to toggle P1 a total of 200 times. Use RAM location 32H to hold your counter value instead of registers R0-R7. (May/Jun 2016)

```
MOV TMOD,#02
MOV 32H, #C8H
MOV TH0, 32H
SETB TR0
L1: CPL P1.0
JNB TF0, L1
CLR TR0
HERE:SJMP HERE
```

PART-B

1.Determine the value of the accumulator after the execution of instructions A:,B:, C: and D:
MOV 40H , #88H
MOV R0 , #40H
A: MOV A , R0
B:MOV A, @R0
C:MOV A, 40H
D: MOV A, #40H

2.With neat diagram explain the timer / counter functions in 8051 Micro Controller.

3.Draw the pin configuration of 8051 and explain the function of each pin in detail.(6)**(May/Jun 2014)**

4.Explain in detail the different addressing modes supported by 8051.(6)

5.Draw the architecture of 8051 and explain? **(Nov/Dec 2016) (May/Jun 2016)**

6.Write an ALP to arrange a set of numbers in descending order.(6)

7.Write a program using 8051 assembly language to add three BCD numbers stored in internal RAM locations 25H, 26H and 27H and put the result in RAM locations 31H (MSB) and 30 H (LSB).Use register R0 to store the intermediate result.

8.List the features of 8051 microcontroller. (8)

9.How do you classify the instruction set of 8051? (8)

10. Explain the I/O structure of 8051 μC.(8) **(Nov/Dec 2013) (May/Jun 2014)**

11. Draw the bit pattern of PSW of 8051 μC and explain the significance of each bit with examples.

12. Write an ALP using 8051 instruction to receive bytes of data serially and put them in P1. Set the baud rate at 4800, 8-bit data and 1 stop bit? **(Nov/Dec 2016)**

13. Write an 8051ALP to create a square wave of 66 % duty cycle on bit 3 of port 1? **(May/Jun 2016)**

14. Explain the internal and external data memory organization of 8051. (10) **(Nov/Dec 2013)**

15. Explain in detail the memory organization of 8051 microcontroller. (16) **(Nov/Dec 2014)**

16. (i) Enumerate about the ports available in 8051 microcontroller. (8)
(ii) Write an assembly language program for 8051 microcontroller to send 20 output pulses at P2.0.Vary the duration of pulse using NOP. (8) **(May/Jun 2014)**

17. (i) Briefly explain the data transfer instructions available in 8051 microcontroller. (8)
(ii) Using timers in 8051 write a program to generate square wave of 100ms, 50% duty cycle. (8) **(Nov/Dec 2014)**

18. (i) Explain in detail about the Special Function Registers in 8051.(8)
(ii) Briefly explain about addressing modes of 8051. (8) **(Nov/Dec 2015)**

19. (i) Give PSW of 8051 and describe the use of each bit in PSW. (8)
(ii) Describe the functions of the following signals in 8051.
RST, EA, PSEN and ALE (8) **(Nov/Dec 2015)**

UNIT-V INTERFACING MICROCONTROLLER

PART-A

1. Compare polling and interrupt? (May/Jun 2016)

When you do a polling, it means you are regularly checking that a bit is set or not. This takes time and you can do a lot of things before checking again and see that the bit actually changed. When working on interruption, the program continues running and do anything it wants and when the event occurs, your software is stopped and execute the interrupt to deal with the event. It means you react immediately to the event and that you don't need to check if the bit is set or not.

2. Write short notes on interrupts in 8051?

Interrupts may be generated by internal chip operations or provided by external interrupts sources. Five interrupts are provided in 8051. Three of these interrupts are generated automatically by internal operations: **Timer flag 0, Timer flag 1, and the serial port interrupts (RI or TI)**. Two interrupts are triggered by external signals provided by the circuitry that is connected to the pins INT0 and INT1 (port pins P3.2 and P3.3).

3. What is the purpose of Interrupt priority (IP) Control register in 8051?

Register IP bits determine if any interrupt is to have a high or low priority. Bits set to 1 give the accompanying interrupt a high priority; a 0 assigns a low priority.If two interrupts with the same priority occur at the same time, then they have the following ranking: IE0, 2.TF0, 3.IE1, 4.TF1,5.Serial = RI or TIFor example, the serial interrupt could be given the highest priority by setting the PS bit in the IP to 1, and all others to 0.

4. What is SBUF?

SBUF stands for SERIAL BUFFER. SBUF is physically two registers. One is write only and is used to hold the data to be transmitted out of the 8051 via TXD. The other one is read only and holds the received data from external sources via RXD. Both mutually exclusive registers use address 99H.

5. What is the basic difference between a timer and a counter?

The only difference between a timer and a counter is the source of clock pulses to the counters.

When used as a timer, the clock pulses are sourced from the oscillator through the divide-by-12d circuit. When used as a counter, pin T0 (P3.4) supplies pulses to counter 0, and pin T1(P3.5) to counter 1.

6. Explain the operating mode 0 of 8051 serial port?

- Mode 0 of 8051 serial port is shift register mode.
- Serial data enters and exits through RXD pin.
- Pin TXD is connected to the internal shift frequency pulse source to supply shift pulses to external circuits.
- 8-bits are transmitted and received.
- The baud rate is fixed at 1/12 of the crystal frequency.

7. Define watch dog timer.

- Watch dog timer is a dedicated timer to take care of system malfunction. It can be used to reset the controller during software malfunction, which is referred to as "Hanging".
- A watchdog timer contains a timer that expires after a certain interval unless it is restarted.
- It resets the microcontroller and starts the software over from the beginning if the software does not restart it periodically.

8. What is the function of the TMOD register?

(Timer mode) register is used to set the various timer operation modes. TMOD is dedicated solely to the two timers (T0 & T1) and can be considered to be two duplicate 4-bit registers, each of which controls the action of the timers.

9. What is the difference between watch dog timer and ordinary timer? (Nov/Dec 2013)

The watch dog timer is provided for the system to check itself and reset if it is not functioning properly. The watch dog register is a 16 bit-counter which is incremented every state time.

10. Define baud rate of 8051? (May/Jun 2016)

The 8051 Serial Port. The 8051 includes an on-chip serial port that can be programmed to operate in one of four different modes and at a range of frequencies. In serial communication the data is rate is known as the baud rate, which simply means the number of bits transmitted per second.

11. What is the significance of BUSY flag in LCD interfacing?

When D7 pin=1 and RS pin=0 the BUSY flag is set which means that LCD is busy taking care of internal operations and will not accept any new information. Therefore we have to check BUSY flag before writing data to LCD.

12. How a pressed key is detected in keyboard interfacing?

The keyboards are organized in a matrix of rows and columns. The microcontroller grounds all rows by providing zero to the output latch then reads the columns.

13. What is the significance of WR and INTR pin in ADC chip?

WR is an active low input and when it undergoes low to high transition the Start of conversion signal is given. INTR is an active low output pin. It is normally high when the A to D conversion is finished. It goes low to signal EOC.

14. Write an ALP to generate a saw tooth waveform.

```
MOV A.#00H
MOV P1,A
BACK: INC A
SJMP BACK
```

15. What is the significance of PSEN in memory interfacing?

PSEN (Program Store Enable) is an output signal for the 8051 microcontroller, which is connected to the OE pin of external ROM containing the program code. This is used when external ROM has to be accessed.

16. What is the relation between RPM and steps per second in stepper motor interfacing?

Steps per second= (rpm × steps per revolution)/60

17. What are the serial communication modes available in 8051?

Mode 0, Mode 1, Mode 2, Mode 3 is the serial communication modes available in 8051.

18. What are the contents of SCON register?

7	6	5	4	3	2	1	0
SMO	SM1	SM2	REN	TB8	RB8	TI	RI

SM0 - Serial port mode bit 0 , SM1 - Serial port mode bit 1, SM2 - Serial port mode 2 bit (or) multiprocessor communication enable bit, REN - Reception Enable bit, TB8 - Transmitter bit 8.
RB8 - Receiver bit 8 or the 9th bit received in modes 2 and 3, TI - Transmit Interrupt flag,
RI - Receive Interrupt flag.

19. What are the various baud rates possible in 8051?

Baud rate	TH1(decimal)	TH1(hex)
9600	-3	FD
4800	-6	FA
2400	-12	F4

20. What is the frame format for mode 2 serial communication?

The 11 bit frame is classified as: 1 bit for start, 8 bits for data, 1 bit can be programmed, 1 bit for stop.

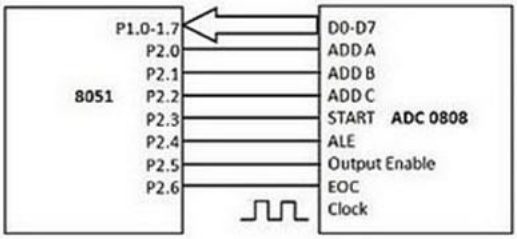
21. Write about the design steps involved in using microcontroller for stepper motor. (May/Jun 2014)

The four leads of the stator winding are controlled by four bits of the 8051 port (P1.0-P1.3). Since the 8051 lacks sufficient current to drive the stepper motor windings, a driver such as ULN2003 is used to energize the stator. The ULN2003 has an internal diode to take care of back EMF.

22. Mention the features of serial port in mode 0. (Nov/Dec 2015)

- Mode 0 of 8051 serial port is shift register mode.
- Serial data enters and exits through RXD pin.
- Pin TXD is connected to the internal shift frequency pulse source to supply shift pulses to external circuits.
- 8-bits are transmitted and received.
- The baud rate is fixed at 1/12 of the crystal frequency.

23. How is A/D converter interfaced with 8051? (Nov/Dec 2015)



One of the most commonly used ADC is ADC0808. ADC 0808 is a Successive approximation type with 8 channels i.e. it can directly access 8 single ended analog signals. ADC0808 has an 8-bit data output. The Microcontroller 8051 is used to provide the control signals to the ADC. The pin P2.0, P2.1 and P2.2 are connected to address pins A, B, and C to select IN0 – IN7, and activate ALE using pin P2.4 to latch in the address. START is for the start of conversion connected pin P2.3. EOC is for end-of-conversion connected to pin P2.6, and OE is for output enable connected to pin P2.5. The port P1 is used as an input port which receives the digital data from the ADC.

24.Define baud rate of 8051usig timer 1.(may 2016(Nov/Dec 2016)

8051 divides the crystal frequency by 12 to get machine cycle frequency. In case of XTAL = 11.0592 Mhz. so machine cycle here becomes 921.6 Khz. Now the 8051 UART circuitry divides the machine cycle frequency of 921.6 Khz by 32 once more before it is used by timer 1 to set the baud rate.So 921.6Khz divided by 32 gives 28,800 hz. This is the value of frequency upon which we will perform operation to get variable baud rate. When timer 1 is used to set baud rate it must be programmed in mode 2 8 bit auto reload.Timer 1 TH1 register values for various baud rates.

25. list of timer modes in 8051?(Nov/Dec 2016)

Mode 0: 13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescalar.
Mode 1: 16-bit timer mode, 16-bit timer/counters THx and TLx are cascaded; There are no prescalar.
Mode 2: -bit auto reload mode, 8-bit auto reload timer/counter; THx holds a value which is to be reloaded into TLx each time it overflows.
Mode 3: Spilt timer mode.

PART-B

1. Describe the different modes of operations of timer/counter in 8051 microcontroller?**(Nov/Dec 2016)**

2. What are the different timer mode operations of 8051? Explain them in detail.

3. Draw an interfacing circuit using 8051 to read the status of 4 thumb wheel switches and display the status in 7 segments LED after 1 min delay. Write an ALP for the same.

4. Discuss the interrupt system of the 8051 μC.(8)

5. Explain how to interface i) ADC and ii) DAC with 8051 μC.(16)

6. Explain how to interface external memory devices with 8051 μC.(8)

7. With necessary h/w & s/w details explain how to interface LCD'S with 8051 μC.(16)

8. Explain the different modes of operation of serial port in 8051, indicating various registers associated with it.(16)

9. Describe the structure of 4 parallel ports in 8051 with necessary diagrams.(16)

10. (i)How do you interface 8051 microcontroller with keyboard? Explain in detail. (8)

(ii) How do you interface 8051 microcontroller with ADC? Explain in detail. (8) **(Nov/Dec 2013)**

(iii) Vin=2.25V, Vref=5V, NO. of data lines are 5. Convert the given analog quantity to its equivalent digital output quantity. (8) **(May/Jun 2014)**

(iv) Explain the different techniques to convert digital quantity to its equivalent analog quantity.

11. Explain in detail the procedure to interface stepper motor with 8051.(8) **(Nov/Dec 2014)**

12. Describe the means to access program code available in external ROM interfaced to 8051.

13. Describe the serial interface with 8051 microcontroller with program. (8) **(May/Jun 2014) (May/Jun 2016)**

14. With a neat circuit diagram explain how a 4x4 keypad is interfaced with 8051 microcontroller and write 8051 ALP for keypad scanning. (16) **(Nov/Dec 2015)**

15. Draw the schematic for interfacing a stepper motor with 8051 microcontroller and write 8051 ALP for changing speed and direction of motor.(16) **(Nov/Dec 2015) (May/Jun 2014) (Nov/Dec 2016)**