DHANALAKSHMI SRINIVASAN COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ECE

CS8351 DIGITAL PRINCIPLES AND SYSTEM DESIGN

Dept/Sem: II CSE/03

UNIT – I BOOLEAN ALGEBRA AND LOGIC GATES
PART – A

1. How many bits are required to represent the decimal numbers in the range 0 to 999 using straight binary code? Using BCD codes?
2. Show that the excess-3 code is self-complementing.
3. How is the letter A coded as in the ASCII code?
4. What is meant by weighted and non-weighted code?
5. Add the decimals 67 and 78 using excess-3 code.
6. Add the decimals 57 and 68 using 8421 BCD code.
7. Write the two properties of Gray code & mention the application of Gray code.
8. Use De Morgan's theorem to convert the following expressions to one that has only single variable inversions?
9. Simplify the expression: X = (A'+B)(A+B+D)D'
10. Write the maxterm for M_{45} using minimum number of variables.
11. Define distributive law.
12. a) Convert $(11001010)_2$ into gray code.
    b) Convert a Gray code 11101101 into binary code.
13. State & prove De-Morgan's theorem.
14. Simplify the expression using Demorgan's theorems Y = [A (B+C') D]'
15. Describe the canonical forms of the Boolean function.
16. Describe the importance of don't care conditions.
17. Write the dual form of F=AB+A'C+BC
18. Simplify Y = (A+B)(A'+C)
19. Give the canonical product form of $F=x_1'x_2'x_3+x_1'x_2x_3'+x_1x_2'x_3'+x_1'x_2x_3$
20. What is a prime implicant?
21. Give the canonical SUM form of F=(x1+x2+x3) (x1'+x2+x3')(x1'+x2'+x3)(x1'+x2'+x3')
22. Define the following: minterm and maxterm.
23. Write the minterm of m_{32} using minimum number of variables.
24. Minimize the function using K-map: F=∑m (1, 2, 3, 5, 6, 7)
25. Find the complement of x+yz.
26. For a switching function of n variables, how many distinct minterms and maxterms are possible?
27. If A and B are Boolean variables and if A=1 and (A+B)' = 0, find B.
28. Express the switching function f (BA) = A in terms of minterms.
29. Apply DeMorgans theorems to simplify (A+BC')'.
29. Define Karnaugh map.
30. Plot the expression on K-map: F (w,x,y) =∑m (0, 1, 3, 5, 6) + d (2, 4)
31. Express x + yz as the sum of minterms
32. Simplify: a) Y = AB'D + AB'D' b) Z = (A'+B) (A+B)
33. Implement OR using NAND only
34. Implement NOR using NAND only
35. What are Universal Gates? Why are they called so?
36. Simplify A+AB+A'+B
37. What are the two forms of Boolean expressions?
38. What are the limitations of karnaugh map?
39. Discuss the NOR operation with a truth table.
40. What is the significance of BCD code?
    (i) Any large decimal number can be easily converted into corresponding binary number

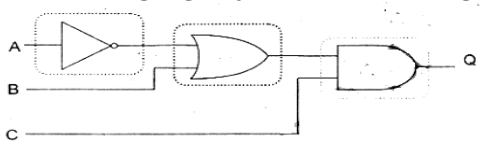
(ii) A person needs to remember only the binary equivalents of decimal number from 0 to 9.
(iii) Conversion from BCD into decimal is also very easy.

41. Realize XOR gate using only 4 NAND gates.
42. State the Principle of Duality.
43.6Implement AND gate using NOR gates.
44. Convert $(0.6875)_{10}$ to binary.
45. Prove the following using DeMorgan's theorem.
46. Convert $(126)_{10}$ to Octal number and binary number.
47. Find the Octal equivalent of the hexadecimal number DC.BA.
48. What is meant by multilevel gates networks?

PART-B

1. Discuss about various codes in digital system.
2. Find the complement of AB'+B'C+CD'
3. What is K-map? Why we need K-maps? Give the various types of K-map.
4. Solve following using K-map and Boolean algebra:
   (i) F(A,B)=∑m(1,3) (ii) F(A,B)=∑m(0,2) (iii) F(A,B)=∑m(1,2)
5. Solve following using K-map and boolean algebra:
   (i) F(A,B,C)=∑m(2,3)(ii) F(A,B,C)=∑m(1,3,5,7) (iii) F(A,B,C)=∑m(0,4,1,3,6)
6. Solve the following using K-map and verify by using boolean algebra: F (A, B, C, D) = ∑m (3, 4, 5,7, 9, 13, 14, 15)
7. Solve the following using k-map:f (A, B, C, D) = ∑m(0,2,3, 8, 1, 12) + d (1,9, 14)
8. Find the maxterms for the expression F=AC'+ABC'+A'BC
9. Construct the truth table for F = XY'+X'Y
10. Convert the given expression in canonical SOP form Y = AC + AB + BC
11. Realize and OR and NOT using NOR gates.
12. Realize X-OR function using NOR gates only.
13. A four-variable function is given as f (A, B, C, D) =∑m (0, 2, 3, 4, 5, 7, 8, 13, 15). Use a K-map to minimize the function.
14. Simplify the expression AB + AC + ABC (AB + C). Implement using minimum number of NAND.
16. A four-variable function is given as f (A, B, C, D) = ∑m (0, 3, 4, 5, 6, 7, 11, 13, 14, 15) Use a K-map to minimize the function.
17. Realize OR, AND, NOT, NOR gates using NAND gates only.
18. Minimize the function using K-map. f (A, B, C, D) = ∑m (0, 1, 2, 3, 5, 7, 8, 9, 11,14) CO114.1
19. Obtain the minimal SOP expression for ∑m (0, 1, 2, 4, 6, 9. 11, 12, 13) and implement it in NAND logic.
20. Obtain the minimal POS expression for π_m (0, 1, 2, 4, 5, 6, 9, 11, 12, 13, 14, 15) and implement it in NOR logic.
21. Simplify the function using Karnaugh map and implement using minimum number of logic gates.
F = (2, 9, 10, 12, 13) + D (1, 5, 14) what are the limitations of Karnaugh map?
22. Minimize the following function by Quine Mccluskey method and list all prime implicants of essential prime implicants. Is the minimum SOP unique, if not all the minimal solutions for the functions?
F (a,b,c,d,e,f) = (0,2,4,7,8,16,24,32,36,40,48) + d (5,18,22,23,54,56)
23. i) Define prime implicant and essential prime implicant.
ii) Procedure logic diagram with NAND gate from Boolean function.
iii) Implement F(x,y,z)= ∑m (1,2,3,4,5,7)with NAND gates.
24. Minimize the following function by Quine Mccluskey method.
Y'=A'BC'D'+A'BC'D+ABC'D'+ABC'D+AB'C'D+A'B'CD'.
25. i) Simplify F(A,B,C,D)= ∑m (0,1,2,5,8,9,10) in SOP, POS using K map.
ii) Write notes on negative/positive logic.
26. Simplify F(A,B,C,D)= ∑m (1,4,6,7,8,9,10,11,15) using QuineMccluskey method. Check if NOR operator is associative.
27. i) State the differences between 1's complement and 2's complement subtraction with examples.
ii) Determine the hamming format for the data 1010.
28.i) State and prove DeMorgan's theorem.
ii) Simplify the following using K-map. F (A, B, C, D) = (3, 4, 5,7, 9, 13, 14, 15)
29. Simlify the following Boolean function F using K-map method.
i) F (A, B, C, D) = ∑m (0,2,4,5,8,14,15) ,d (A, B, C, D)= ∑m (7,10,13)
ii) F (A, B, C, D) = ∑m (4,6,7,8,12,15) ,d (A, B, C, D)= ∑m (2,3,5,10,11,14)

30. Simlify the following Boolean function F using Tabulation method.
i) F (A, B, C, D) = ∑m (0,6,8,13,14) ,d (A, B, C, D)= ∑m (2,4,10)
ii) F (A, B, C, D) = ∑m (1,3,5,7,9,15) ,d (A, B, C, D)= ∑m (4,6,12,13)
31. Reduce the following function using K-map technique.
i) f (A, B, C) = ∑m (0,1,3,7) + ∑d (2,5)
ii) F (w,x,y,z) = ∑m (0,7,8,9,10,12) + ∑d (2,5,13)
32. Simplify the Boolean function using Quine McCluskey method:
F (A, B, C, D,E,F) = ∑m (0,5,7,8,9,12,13,23,24,25,28,29,37,40,42,44,46,55,56,57,60,61)
33. Simplify the Boolean function using Quine McCluskey method:
F (A, B, C, D,E) = ∑m (0,1,3,7,13,14,21,26,28) + ∑d(2,5,9,11,17,24)
34. i) Simplify the given Boolean function in POS form using K-map and draw the logic diagram using only NOR gates. F(A,B,C,D)= ∑m (0,1,4,7,8,10,12,15)+d(2,6,11,14)
ii)Convert 78.5_{10} into binary.
ii) Find the dual and complement of the following Boolean expression.
Xyz'+x'yz+z(xy+w).
35. Simplify the following functions using K-map technique
G=∑m (0,1,3,7,9,11) (ii) f(w,x;y,z)=∑m(0,7,8,9,10,12)+∑d(2,5,13)
36. Minimize the expression usinequineMccluskey(tabulation) method
F=∑m(0,1,9,15,24,29,30) +∑d(8,11,31)
37. Simplify the function F(w,x,y,z) = ∑m(2,3,12,13,14,15) using tabulation method. Implement the simplified function using gates.
38. i) Simplify the Boolean function in Sum of Products (SOP) and Product of sums (POS)
F(A,B,C,D) = ∑m(0,1,2,5,8,9,10)
ii) Plot the following Boolean function in Karnaugh map and simplify it.
F(w,x,y,z) = ∑m(0,1,2,4,5,6,8,9,12,13,14)
39. Simplify the following Boolean expression in
(i) Sum-of-product
(ii) Product-of-sum using Karnaugh-map
AC′+B′D+A′CD+ABCD
40. (i) Express the following function in sum of min-terms and product of max-terms
F(x,y,z) = x+yz.
(ii) Convert the following logic system into NAND gates only.



41. Simplify the following switching functions using Karnaugh map method and realize expression using gates *F(A,B,C,D) = Σ(0,3,5,7,8,9,10,12,15).*
42. Simplify the following switching functions using Quine McCluskey's tabulation method and realize expression using gates F(A,B,C,D) = Σ(0,5,7,8,9,10, 11, 14,15).
43. Reduce the expression using Quine McCluskey's method F(x_1, x_2, x_3, x_4, x_5) = ∑m (0, 2, 4, 5, 6, 7, 8, 10, 14, 17, 18, 21, 29, 31) + ∑d (11, 20, 22)
44. Determine the MSP form of Switching function F (a, b, c, d) = ∑m (0, 2, 4, 5, 6, 8) + ∑d (10, 11, 12, 13, 14, 15)

UNIT-II COMBINATIONAL LOGIC
PART - A

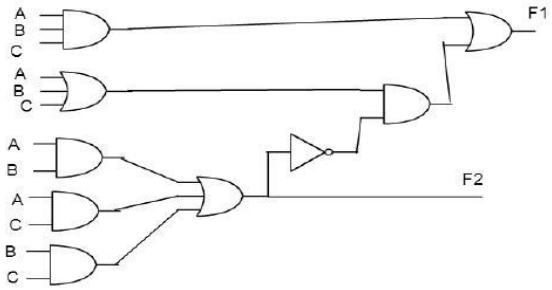
1. Draw the 4 bit Gray to Binary code converter.
2. Draw the 4 bit Binary to Gray code converter
3. Distinguish between combinational logic and sequential logic.
4. Implement half Adder using NAND Gates.
5. Design a half subtractor.
6. How many binary outputs would a 3 digit BCD-to-Binary converter have?
7. Define Combinational circuit?
8. What is an ALU?
9. Give the truth table for half adder and write the expression for sum and carry?

10. Obtain the expression for sum and carry output of a full adder and implement the same.
11. Obtain an expression for difference and borrow outputs of a full subtractor.
12. Draw the logic circuit for the expression F=A'B+AB'C'
13. Draw the logic circuit for the expression F=x'y'z+x'yz'+xy'
14. Using a single IC 7485, draw the logic diagram of a 4-bit comparator.
15. What is a half-adder?
16. What is a full-adder?
17. What is half-subtractor?
18. What is a full-subtractor?
19. What is Binary parallel adder?
20. Give some of the major applications of multiplexers.
21. What is a priority encoder?
22. Define SSI and MSI.
23. List the applications of decoders.
24. Mention the difference between a DEMUX and a MUX
25. Implement the following Boolean function using 8:1 multiplexer.
    $F(A,B,C) = \sum m(1,3,5,6)$
26. Write the Data flow description of a 4-bit Comparator.
27. Draw the truth table of half adder.
28. Define Combinational circuits.
29. Design the combinational circuit with 3 inputs and 1 output. The output is 1 when the binary value of the input is less than 3. The output is 0 otherwise.
30. Implement a full adder with 4 x 1 Multiplexer.
31. Draw the logic diagram of a one to four line demultiplexer.
32. Draw the logic diagram of a one to four line de-multiplexer.
33. Draw a 2 to 1 multiplexer circuit.
31. Give functional block diagram of 2 1 MUX
32. Distinguish between a decoder and a demultiplexer.
33. Define Tristate gates.
34. Implement a full adder with two half adder.
35. Implement a 4 bit even parity checker.
36. Implement a 4 bit even parity generator.
37. Write HDL behavioral description of 4 bit comparator with 6 bit output y[5:0].
38. Write down the truth table of a full subtractor.
39. Obtain the truth table for BCD to Excess-3 code converter
40. Draw the truth table and circuit diagram of 4 to 2 encoder.

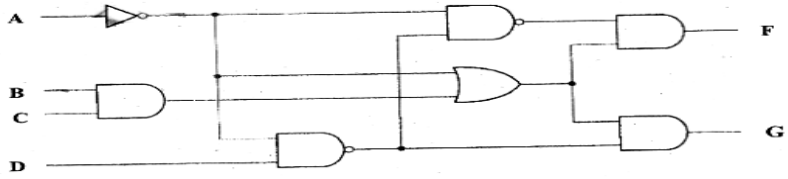
PART - B

1. Design 3 bit Gray Code to binary converters
2. Design BCD to Excess-3 code converter.
3. Design full subtractor using NAND gates.
4. Design a Gray-to Excess-3 Code converter using NAND gates
5. Discuss the need and working principle of Carry Look ahead adder.
6. Draw the circuit of a 3 bit binary subtractor and explain its operation with the help of an example.
7. Design a Gray to Excess-3 code converter using NOR gates.
8. Design the circuit for one bit comparator.
9. Design a full adder circuit using NAND gates only
10. Design a combinational circuit to perform BCD addition.
11. Write note on 3 bit binary magnitude comparator.
12. Realize the circuit of a full adder in terms of two half adders from its truth table.
13. What are Magnitude comparators" Explain the design of magnitude comparators with the help of a suitable example
14. Construct 16-bit comparator using 4-bit comparator as a building block.
15. Design Half/Full Subtractor circuits.
16. Design 8421 BCD code to Excess 3 code.

17. i) Analyze the circuit: give truth table and Boolean expression.
    ii)Explain BCD adder.



18. i) Design BCD to excess 3 code.
    ii) Draw 4 bit adder/subtractor using full adder.
19. Implement half adder circuit using 4: 1 MUX or multiplexers only.
20. Implement using 4: 1 MUX F= ∑m(0,3,4,7)
21. Draw the logic circuit for the expression F=A'B+AB'C'
22. Draw the logic circuit for 3 line to 8 line decoder
23. Draw the logic circuit for the expression F=x'y'z+x'yz'+xy'
24. How many select lines are there for a 30 to 1 MUX?
25. Describe the operations performed by an encoder and a decoder.
26. Implement the function using 3 to 8 decoder f(A,B,C)= ∑m(0,1,4,5,7)
27. Define a demultiplexer Show how to convert a decoder into a demultiplexer indicate how to add a strobe to this system
28. Give the logic diagram of 4-to-2 encoder and explain its importance in design of digital system.
29. Use a 8 x 1 MUX to implement the logic function F=∑m (0,1,2,3,4,10,11,14,15)
30. Implement F(A,B,C,D)= ∑m (1,3,4,11,12,13,14,15) using 8X1 mux.
31. Design 4 bit priority encoder.
32. Briefly explain about HDL.
33. Write HDL for the expression. x = A.B + C1 y = C1
34. Write HDL for MUX in behavior mode.
35. i) Design full adder using NAND gates.
    ii) Design a 4-bit 2's complement circuit.
36. i) Design a 4-bit Binary to Excess-3 code converter.
    ii) Design a BCD Adder using two 4-bit parallel binary adder blocks and additional logic.
37. i) Design a priority encoder and explain its operation.
    ii) Implement full adder using suitable decoder and additional logic.
38. Design a BCD to 7 segment decoder and implement it by using basic gates.
39. Construct a 4 to 16 line decoder with an enable input using five 2 to 4 line decoders with enable input.
40. Design a full adder using 2 half adders.
41. Design a combinational circuit to convert binary to gray code.
42. Implement the switching function F=∑m (0, 1, 3, 4, 12, 14, 15) using an 8 input mux.
43. i) Design a 4-bit magnitude comparator with three outputs: A>B, A=B & A<B.
    ii) Construct a 4-bit odd parity generator circuit using gates.
44. i) Realize 4 x 16 decoder using two 3 x 8 decoders with enable input.
    ii) Implement the following function using a multiplexer. F(W,X,Y,Z)= ∑m (0,1,3,4,8,9,15)
45. (a) Design a circuit that converts 8421 BCD code to Excess-3 Code
    (b) Implement the following using 8 to 1
    F (A, B, C, D) =A'BD'+ACD+B'CD+A'C'D. Also implement the function using 16 to 1 multiplexer
46. Design and Implement a 8421 to gray code converter. Realize the converter using only NAND gates.
47. Design 2-bit Magnitude Comparator and write a Verilog HDL code.
48. (i) Implement the following Boolean functions with a multiplexer:
    F(w,x,y,z) = ∑ (2,3,5,6,11,14,15)
    (ii) Construct a 5 to 32 line decoder using 3 to 8 line decoders and 2 to 4 line decoder.
49. (i) Explain the Analysis procedure. Analyze the following logic diagram.



    (ii) With neat diagram explain the 4-bit adder with carry lookahead.

50. Design a full subtractor and derive expression for difference and borrow. Realize using gates.
51. Design a code converter thet converts a 8421 to BCD code.
52. Design a full adder with x, y, z and two outputs S and C. The circuits performs x+y+z, z is the input carry, C is the output carry and S is the Sum.
53. Design a logic circuit that accepts a 4 bit Gray code and converts it into 4 bit binary code.
54. Implement the following Boolean function with 4 X 1 multiplexer and external gates. Connect inputs A and B to the selection lines. The input requiremnts for the four data lines will be a function of variables C and D these values are obatined by expressing F as a function of C and D for each four cases when AB = 00, 01, 10 and 11. These functions may have to be implemented with external gates.
$F(A, B, C, D) = \Sigma (1, 2, 5, 7, 8, 10, 11, 13, 15)$.

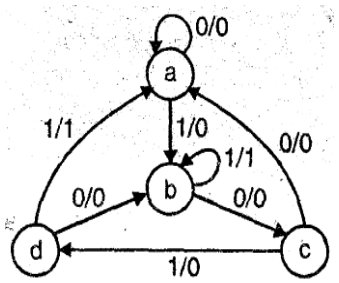
UNIT – III SYNCHRONOUS SEQUENTIAL LOGIC
PART - A

1. What type of FF is best suited for synchronous transfer?
2. What is meant by the term edge triggered?
3. How do you define Excitation table?
4. Give the truth table for J-K flip-flop
5. Show D flip-flop implementation from a J-K flip-flop
6. Give the excitation table of J-K flip flop.
7. Write the characteristics table of a D flip flop.
8. Show the T-Flipflop implementation from SR flipflop
9. With reference to a JK flip-flop, what is racing?
10. Define the hold time requirement of a clocked FF?
11. What is meant by triggering of Flip flop?
12. Differentiate between Flip flop & Latch.
13. Give the truth table of T flip flop.
14. Why is parallel counter referred to as synchronous?
15. Why D FF is known as Delay FF?
16. Name the two problems that may arise in ripple counters or asynchronous counters.
17. When is a counter said to suffer from lockout?
18. Distinguish between synchronous and asynchronous counters.
19. Mention why the decoding gates for an asynchronous counter may have glitches on their outputs?
20. Draw a Mod 6 counter using feedback technique.
21. What is a self-correcting counter?
22. State how an asynchronous down counter differs from an up counter circuit.
23. What is a ripple counter?
24. What is the minimum number of flip-flops needed to build a counter of modulus 60?
25. What is a universal shift register?
26. A shift register comprises of JK flip-flops. How will you complement the contents of the register?
27. If a serial-in-serial-out shift register has N stages and if the clock frequency is f, what will be the time delay between input and output?
28. Mention the uses of shift registers.
29. What are Mealy and Moor machines? (or) Distinguish Moore and Mealy circuit.
30. What is a state diagram?
31. What is finite state machine?
32. What do you meant by the term state reduction problem?
33. Define Bit time & Word time.
34. Give applications of J-K flip-flops.
35. How race around condition can be eliminated?
36. Give application of D and T flip-flops.
37. How many flip-flops are required to count 16 clock pulses? Why?
38. Give difference between latch and flip-flop.
39. Differentiate between sequential and combinational circuits.
41. Write the characteristics table and equation of JK flip flop.
42. How many flip flops are required to realize MOD 50 counter?

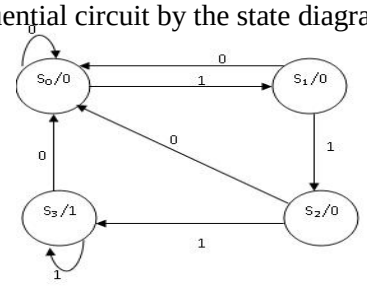
43. What is a ring counter?
44. What is a Mealy circuit?
45. How many states are there in a 3-bit ring counter? What are they?
46. Write the HDL code for up-down counter using behavioral model.
47. Give the block diagram of Master-Slave D flip-flop.
48. Write short notes on propagation delay.
49. Draw the diagram of T flip flop and discuss its working.
50. State the excitation table of JK Flip Flop.

PART-B

1. Explain T-flip-flop with suitable internal structure.
2. Convert SR flip-flop to T flip-flop.
3. For the given state diagram, draw the state reduction diagram. Stats Diagram:



4. Why gated D latch is is called transparent latch? Explain with the logic diagram.
5. Give the truth-table for each flip-flop type: (a) J-K ; (b) D ; and (c) T
6. Draw logic circuit diagram for 3-bit synchronous up-down counter with clear input, start input and 'done' output. The counter should produce 'done' output after completion of counter in either direction.
7. Draw the logic circuits and the excitation tables for the T, JK flip-flops.
8. Classify the sequential circuits.
9. Describe the difference between a gated S-R latch and an edge-triggered S-R flip flop.
10. What is the difference between level and edge triggering? Explain the working of master slave J-K flip flop.
11. Draw a master-slave J-K flip-flop system. Explain its operation and show that the race-around condition is eliminated.
12. Explain what is universal shift register? Explain its working.
13. Draw the logic symbols for T and RS flip-flops. Explain the function of each type of flip-flop.
14. Draw the circuit of an S-R flip-flop using NAND gates. Modify it to include clock Derive J-K circuit from SR flip-flop circuit and explain its truth table
15. Design a J-K counter that goes through states 2, 4, 5, 7, 2, 4…… is the counter-self starting.
16. Perform the following conversions T flip-flop to D flip-flop.
17. Design a synchronous decade counter to count in the following sequence 1,0,2,3,4,8,7,6,5
18. Write short note on the following: Counter design with state equation and state diagrams.
19. What is race around condition in J-K flip flop? How it is eliminated?
20. Write note on: 4 bit binary shift register.
21. Design a BCD counter using JK flip-flops. (or) Design a MOD-10 Synchronous counter using JK flip-flops. Write execution table and state table.
22. Design an up-down counter using JK Flip-flop to count 0, 2, 3, 6, 4, 0….
23. Design an up-down *counter* using D-flip-flops to count 0, 3, 2, 6, 4, 0,.....
24. i) Draw a 4 bit ripple counter with D flip flop. ii) Write the HDL for the above circuit.
    Design 3 bit binary counter.
    ii) Write HDL of T flip flop and JK flip flop from D flip flop.
25. Design sequential circuit by the state diagram using JK flip flop.



26. Design a sequential circuit using RS flip flop for the state table with minimum flip flop.

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	G	F	0	1
G	A	F	0	1

27.i) Explain the operation of a JK Master Slave flip flop with logic diagram.
ii) Design a counter that goes through the following sequence of states: 0,3,2,4,1,5,7,0,3,2.

28. Design a 4-bit parallel in serial out shift register.

29. Design synchronous mod 16 counter using JK flip flop.

30. i) Write behavioural VHDL Description of 8 bit shift register with direct reset.
ii) What is the difference serial and parallel transfer? Explain how to convert parallel data to serial and serial data to parallel. What type of register is needed?

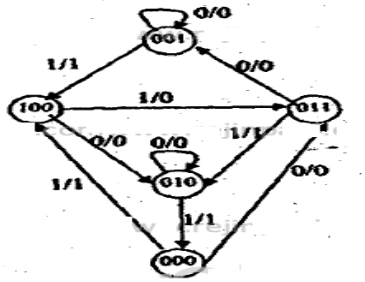
31. Design a shift register using JK flip flops.

32. Using D flip flops, design a synchronous counter which counts in the sequence, 000,001,010,011,100,101,110,111,000,...

33. Design a synchronous counter with the following sequence: 0,1,3,7,6,4 and repeats. Use JK flip flop.

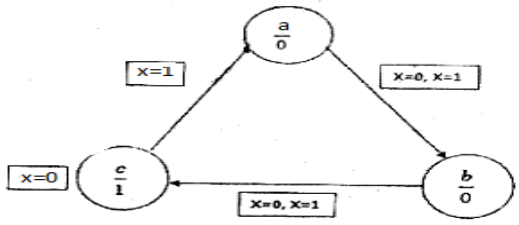
34. Design a synchronous counter that counts the sequence 000,001,010,011,100,101,110,111,000 using D flip flop.

35. Design a sequential circuit by the following state diagram using T-flip flops



36. Implement T flipflop using D flipflopand JK flipflop using D flipflop.

37. (i) How race condition can be avoided in a flip flop.
(ii) Realize the sequential circuit for the state diagram shown below.



38. i) A sequential circuit with two D flip-flops A and B, one input x and one output z is specified by the following next-state and output equations:
A(t+1)= A′+B, B(t+1)=B′x, z=A+B′
(1) Draw the logic diagram of the circuit
(2) Draw the state table
(3) Draw the state diagram of the circuit
ii) Explain the difference between a state table, characteristics table and excitation table.

39. Consider the design of 4-bit BCD counter that counts in the following way:
0000,0010,0011,….,1001 and back to 0000
(i) Draw the state diagram
(ii) List the next state table
(iii) Draw the logic diagram of the circuit

40. Design a sequence detector that detects a sequence of three or more consecutive 1’s in a string of bits

coming through an input line and produces an output whenever this sequence is detected.
41. Design three bit synchronous counter with T flip flop and draw the diagram.
42. Design a binary counter using T flip flops to count in the following sequences:
    (i) 000, 001, 010, 011, 100, 101, 111, 000
    (ii) 000, 100, 111, 010, 011, 000
43. Design a modulo 5 synchronous counter using JK Flip Flop and implement it. Construct its timing diagram.

UNIT- IV ASYNCHRONOUS SEQUENTIAL LOGIC

PART – A

1. What is asynchronous sequential circuit?
2. Why is the pulse mode operation of asynchronous sequential circuits not very popular?
3. What is the difference between synchronous and asynchronous sequential circuits?
4. Mention the applications of Asynchronous circuits.
5. What do you mean by Race condition?
6. Explain the fundamental mode of operation.
7. Distinguish between fundamental mode circuits and pulse-mode circuits.
8. What are Latches?
9. Define Flow table.
10. Explain non- critical race.
11. Explain critical race.
12. Define the term Maximal compatible
13. Define closed covering.
14. Explain Shared Row method.
15. Define Merger diagram.
16. Explain Multiple row method.
17. What is a hazard? (or) Define hazard.
18. Differentiae Static & Dynamic Hazard.
19. Explain Hazards in sequential circuits.
20. Define Essential Hazard.
21. Explain the use of SR latches in asynchronous sequential circuits.
22. What is Primitive Flow table?
23. What do you understand by the term merging?
24. What is finite state Machine?
25. Define critical race in asynchronous sequential circuits.
26. What is meant by debouncing switch?
27. What is State Assignment?
29. What is the need of state reduction in sequential circuit design?
30. What is the use of flip-flop excitation table?
31. What is dynamic hazard?
32. What is state machine?
33. What is the reason for essential hazard to occur?
34. Define compatible states.
35. When is a sequential machine said to be strongly connected?
36. What is One-Hot assignment?
37. What is the difference between an internal state and a total state?
38. Explain the difference between the stable state and the unstable state.
39. Define cycle.
40. What is ASM chart?
41. What are static ‘1’ and static ‘0’ hazards?
42. What are cycles and races?
43. Give the block diagram of asynchronous sequential circuit.
44. What are the different types of shift type?
45. What are the types of hazards?
46. What is critical race condition? Give example.

47. What is race condition?
48. What is lockout? How is avoided?
49. Define the critical race and non critical race.

UNIT -V MEMORY AND PROGRAMMABLE LOGIC
PART – A

1. Define Bit time & Word time.
2. What is PLA and Its uses?
3. Define Bit time & Word time.
4. What is non- volatile memory?
5. What does burning a ROM mean?
6. How long will it take to erase UV erasable EPROM completely?
7. What is the difference between PROM and PLA?
8. What are the major drawbacks of the EEPROM?
10. How many data inputs, data outputs and address inputs are needed for a 1024 x 4 ROM?
11. Describe the basic functions of ROM and RAM
12. Distinguish between PAL and PLA.
13. What is Configurable Logic Block?
14. Give the different types of RAM.
15. What is dynamic RAM cell? Draw its basic structure.
16. What is Memory refresh?
17. What do you mean by PLD's?
18. Define ASIC.
19. What is memory decoding?
20. What is the difference between PAL and PLA?
21. Where do we use PLA's?
22. Compare SRAM and DRAM.
23. Whether PAL is same as PLA? Explain.
24. What is a volatile memory? Give example.
25. How to detect double error and correct single error?
26. Differentiate between EEPROM and PROM.
27. What is memory address register?
28. Write short notes on PLA.
29. A seven bit Hamming code is received as 1111110. What is the correct code?
30. Draw the waveforms showing static 1 hazard?

PART-B

1. Implement the Boolean function using PAL. Y1=$\sum$m(1,3,5,7), Y2=$\sum$m(2,4)
2. Design half adder circuit using PLA.
3. What is PAL?
4. Describe with diagram internal architecture of PLA
5. The difference between static and dynamic memories.
6. Give the classification of memories.
7. A certain memory stores 8 k x 16 bit words. How many data input lines, data output lines and address lines does it have? What is its capacity in bytes?
8. What are the various types of ROMs? Discuss their relative advantages and disadvantages.
9. State and explain the difference among ROM, PROM, RAM, SRAM and DRAM.
10. Write short note on Classification and characteristics of memories.
11. Explain the architecture and function of programmable logic arrays
12. Implement using PLA A(x,y,z)= $\sum$m (1,2,4,6) B(x,y,z)= Σ_m (0,1,6,7) C(x,y,z)= $\sum$m (2,6).
13. Implement a full adder with two 4X1 Mux.
14. i) Write short notes on PLA/PAL. ii) Write notes on RAM its operation and types.
15. i) Explain the operation of a Static RAM.
    ii) Implement the following function using PAL: f(A,B,C,D)= Σ_m (0,2,4,6,8,10,12,14)
16. With suitable example explain how combinational circuits are implemented using Programmable logic arrays.
17. Implement the switching functions.
    Z1=ab'd'e+a'b'c'd'e'+bc+de

Z2=a’c’e

Z3=bc+de+c’d’e’+bd

Z4=a’c’e+ce using 5 x 8 x 4 PLA

18.i) Implement the following Boolean functions using 8 x 2 PROM.

F1= ∑m (3,5,6,7) and F2= ∑m (1,2,3,4)

ii) Implement the following Boolean functions using PLA with 3 inputs, 4 product terms and 2 outputs.

‘ F1= ∑m(3,5,6,7) and F2= ∑m (1,2,3,4)

19. Implement the following function using PLA

A(x,y,z)= ∑m(1,2,4,6) B(x,y,z)= ∑m(0,1,6,7) C(x,y,z)= ∑m(2,6)

20. The following messages have been coded in the even parity hamming code and transmitted through a noisy Channel. Decode the messages, assuming that at most a single error has occurred in each code word.

(i)1001001 (ii)0111001 (iii)1110110 (iv)0011011

21. Design a BCD to Excess-3 code converter and implement using suitable PLA.

22. Discuss on the concept of working and applications of semiconductor memories.

23. (i) Write short notes on Address multiplexing.

(ii) Briefly discuss the sequential programmable devices.

24. (i) Implement the following two Boolean functions with a PLA

F1=AB′+AC+A′BC′

F2=(AC+BC)′

(ii) Give the internal block diagram of 4x4 RAM.

25. Implement the following function using PAL F1 (A, B, C) = Σ(1, 2, 4, 6); F2 (A, B, C) = Σ(0, 1, 6, 7); F3 (A, B, C) = Σ(1, 2, 3, 5, 7).

26. Design a combinational circuit using ROM that accepts a three bit binary number and outputs a binary number and outputs a binary number equal to the square of the input number.